IRT Eurocard

Types DDC-3260, DDC-3270 & DDC-3275

MPEG Transport Stream Adapters

Telstra Serial/Items
347/121 - DDC-3260
347/122 - DDC-3270
347/123 - This manual.

Designed and manufactured in Australia

IRT Eurocard

Types DDC-3260, DDC-3270 & DDC-3275

MPEG Transport Stream Adapters

Instruction Book

Table of Contents

This instruction book applies to units later than S/N 9800000.

General description

The DDC-3260, 3270, 3275 and 3320 form a family of data transcoders for converting between the commonly used MPEG2 Transport Stream formats by the broadcast industry for video distribution.

These formats include:

SPI (Synchronous Parallel Interface MPEG2)
Unframed G.703 HDB3 34 Mb/s
Unframed G.703 B3ZS 45 Mb/s
ASI-C (Asynchronous Serial Interface 270 Mb/s Coaxial cable)
ASI-O (Asynchronous Serial Interface 270 Mb/s Fibre optic cable)
Serial Data plus Clock

The adapters find particular application in CATV Headends where equipment from different manufacturers uses different formats. They may also be used for monitoring connections to test equipment.
In addition, the DDC-3270 & DDC-3271 provide facilities for changing certain coding features of the MPEG transport stream to ensure compatibility between signals.

The individual module features are summarised below:

Input	Simultaneous outputs
DDC-3260:	
Unframed G.703 HDB3 34 Mb/s	SPI Unframed G.703 HDB3 at input rate. ASI-O ASI-C Serial Data plus Clock

The DDC-3260 transcodes the G.703 input and monitors the signal for MPEG2 transport stream sync errors. It does not alter the base coding of the MPEG2 transport stream.
The DDC-3260 G.703 output is unframed HDB3 at 34 Mb/s only. The G.703 input data rate must be 34 Mb/s to produce a G.703 output at 34 Mb/s.

DDC-3261:	
Unframed G.703 B3ZS 45 Mb/s	SPI Unframed G.703 B3ZS at input rate. ASI-O ASI-C Serial Data plus Clock

The DDC-3261 performs the same functions at the 45 Mbit/s G.703 rate as the 34 M/bit/s DDC-3260.
In addition the DDC-3261 G.703 output may be selected as shaped or unshaped. The G.703 input data rate must be 45 Mb/s to produce a G.703 output at 45 Mb/s.

Input	Simultaneous outputs
DDC-3270:	
SPI 22 Mb/s to 48 Mb/s (Nominal 34 Mb/s)	SPI Unframed G.703 HDB3 at input rate. ASI-O ASI-C

The DDC-3270 allows Reed Solomon correction and the insertion or removal of interleaving and MPEG2 transport stream spectrum shaping randomisation. This makes it an ideal adjunct to test equipment or for matching signal from various sources using different encoding options.
The DDC-3270 G.703 output is unframed HDB3 at 34 Mb/s only. The SPI input data rate must be 34 Mb/s to produce a G.703 output at 34 Mb/s.

DDC-3271:	
SPI 22 Mb/s to 48 Mb/s (Nominal 45 Mb/s)	SPI Unframed G.703 B3ZS at input rate. ASI-O ASI-C

The DDC-3271 performs the same functions at the 45 Mbit/s data rate as the 34 Mbit/s DDC-3270.
The DDC-3271 G.703 output is unframed, unshaped G.703 B3ZS at 45 Mb/s only. The SPI input data rate must be 45 Mb/s to produce a G.703 output at 45 Mb/s.

DDC-3275:	
SPI 22 Mb/s to 48 Mb/s. (Nominal 34 Mb/s)	Serial Data plus Clock Unframed G.703 HDB3 at input rate. ASI-O ASI-C

The DDC-3275 transcodes the SPI input and monitors the signal for MPEG2 transport stream sync errors. It does not alter the base coding of the MPEG2 transport stream.
The DDC-3275 is the direct inverse of the DDC-3260. The DDC-3270 provides similar conversion capability, but with the added complexity of coding options and without a Serial Data plus Clock output.
The DDC-3275 G.703 output is unframed HDB3 at 34 Mb/s only. The SPI input data rate must be 34 Mb/s to produce a G.703 output at 34 Mb/s.

DDC-3276:	
SPI 22 Mb/s to 48 Mb/s. (Nominal 45 Mb/s)	Serial Data plus Clock Unframed, unshaped G.703 B3ZS at input rate. ASI-O ASI-C

The DDC-3276 performs the same functions at the 45 Mbit/s data rate as the 34 Mbit/s DDC-3275.
The DDC-3276 G.703 output is unframed, unshaped G.703 B3ZS at 45 Mb/s only. The SPI input data rate must be 45 Mb/s to produce a G.703 output at 45 Mb/s.

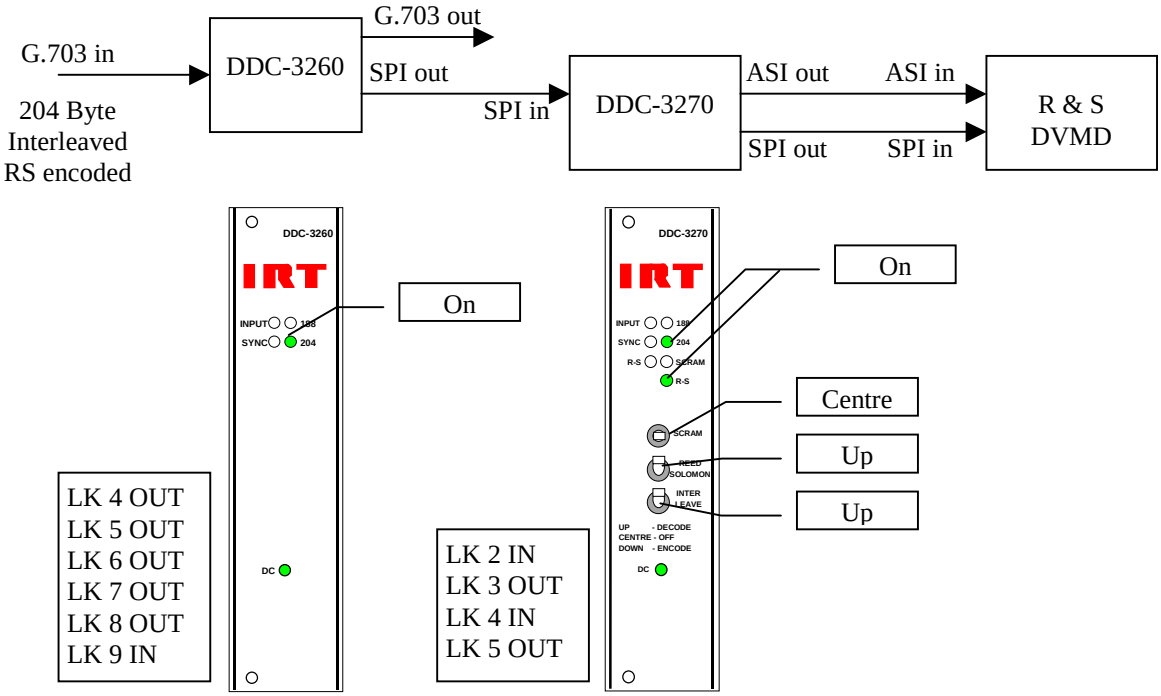
Applications:

- **Block length indication and error detection.**
- **Conversion from cable to fibre.**
- **Interface to test equipment.**
- **Interfacing various MPEG2 TS formats.**
- **Interleaving or de-interleaving. ***
- **Reed Solomon insertion & correction. ***
- **Spectrum dispersion correction. ***
- **Signal monitoring for remote alarm indications.**

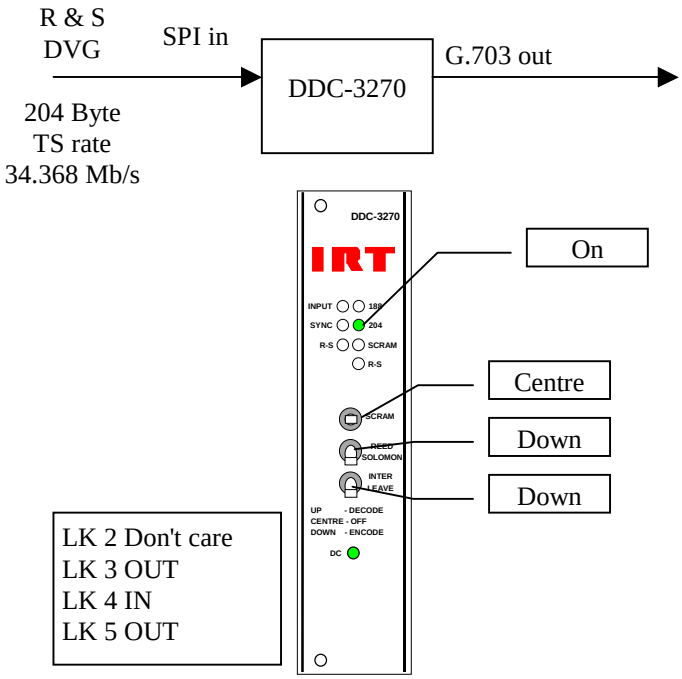
* DDC-3270 & DDC-3271 only.

Application examples

Telstra / Foxtel TS decoder:



Telstra / Foxtel TS formatting:



Cable System application

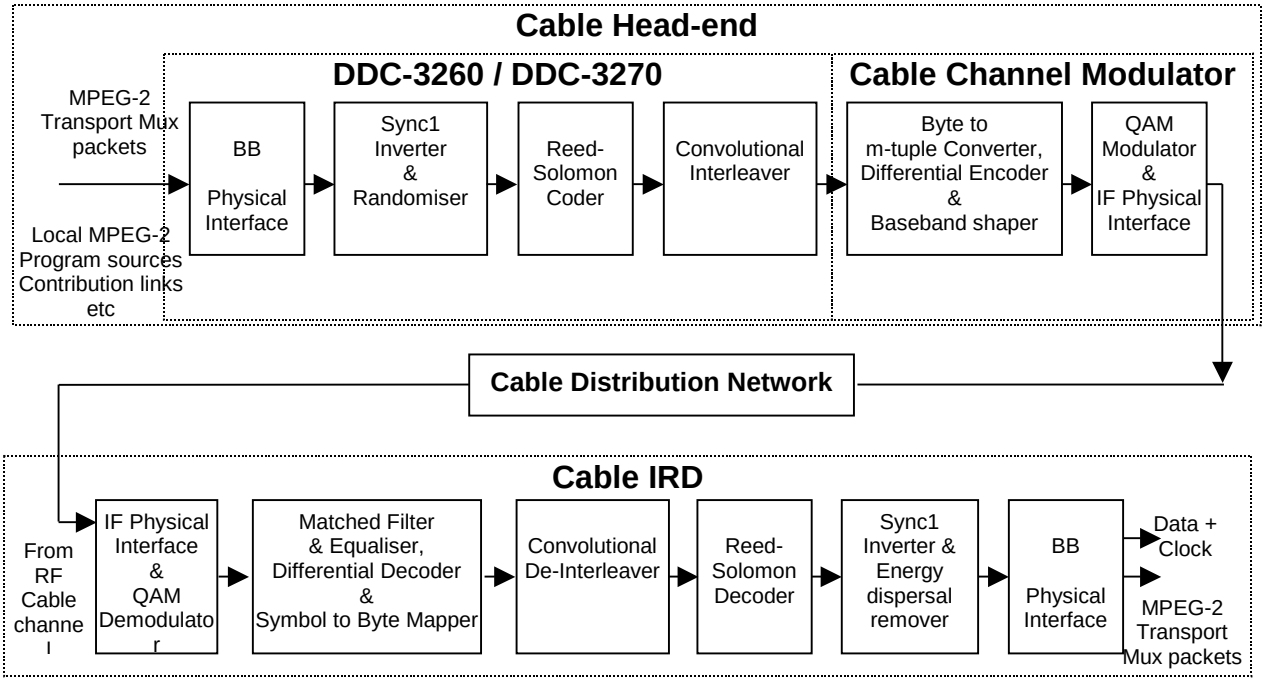
For detailed standards and specifications see ETS 300 429.

In a cable system equipment is required that adapts baseband TV signals to the cable channel characteristics.
In the cable head-end, the following TV baseband signal sources may be present:

satellite signal(s)
contribution link(s)
local program source(s).

These signals need to be formatted in the same way before being passed to the cable channel modulator. The DDC-3270 performs these functions. In certain cases the DDC-3260 may be used to precede the DDC-3270 in order to provide compatibility with G.703 sources.

The following diagram shows a summary of the processes involved. A cable receiver is shown to provide a better understanding of the complete system.



Processes which may be performed by the DDC-3260 / DDC-3270 are:

Baseband interfacing and sync

This unit adapts the data structure to the format of the signal source. This may be a DDC-3260 or simply the input interface of the DDC-3270. The framing structure is in accordance with MPEG-2 transport layer including sync Bytes.

Sync 1 inversion and randomisation (Scrambling)

The Sync 1 Byte is inverted according to the MPEG-2 framing structure, and the data stream randomised for spectrum shaping purposes.

Reed-Solomon (RS) encoder

A shortened Reed-Solomon (RS) code is applied to each randomised transport packet to generate an error-protected packet. This code is also applied to the Sync Byte itself.

Convolutional interleaver

This part performs a depth I = 12 convolutional interleaving of the error-protected packets. The periodicity of the sync Bytes remains unchanged.

The other processes, which are not performed by the DDC-3260 / DDC-3270 are:

Byte to m-tuple conversion

This unit performs a conversion of the Bytes generated by the interleaver into QAM symbols.

Differential encoding

In order to get a rotation-invariant constellation, this unit applies a differential encoding of the two Most Significant Bits (MSB's) of each symbol.

Baseband shaping

This unit performs mapping from differentially encoded m-tuples to I and Q signals and a square-root raised cosine filtering of the I and Q signals prior to QAM modulation.

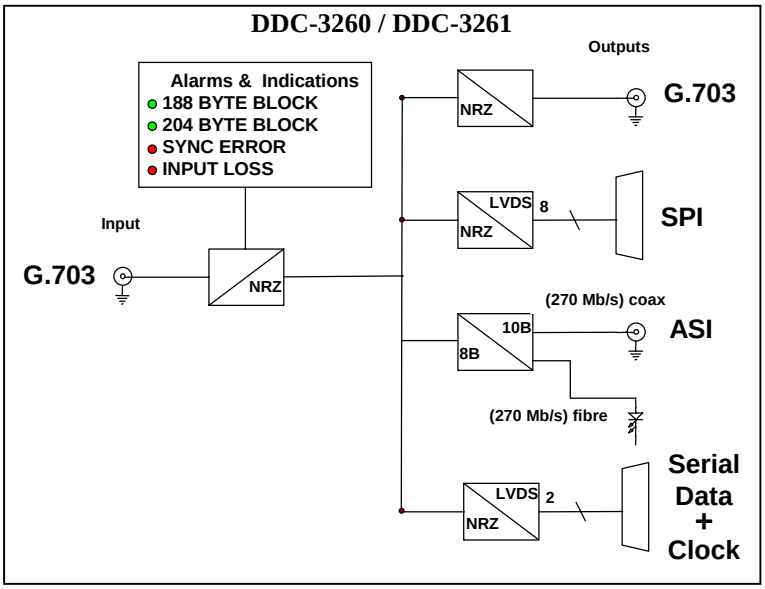
QAM modulation and physical interface

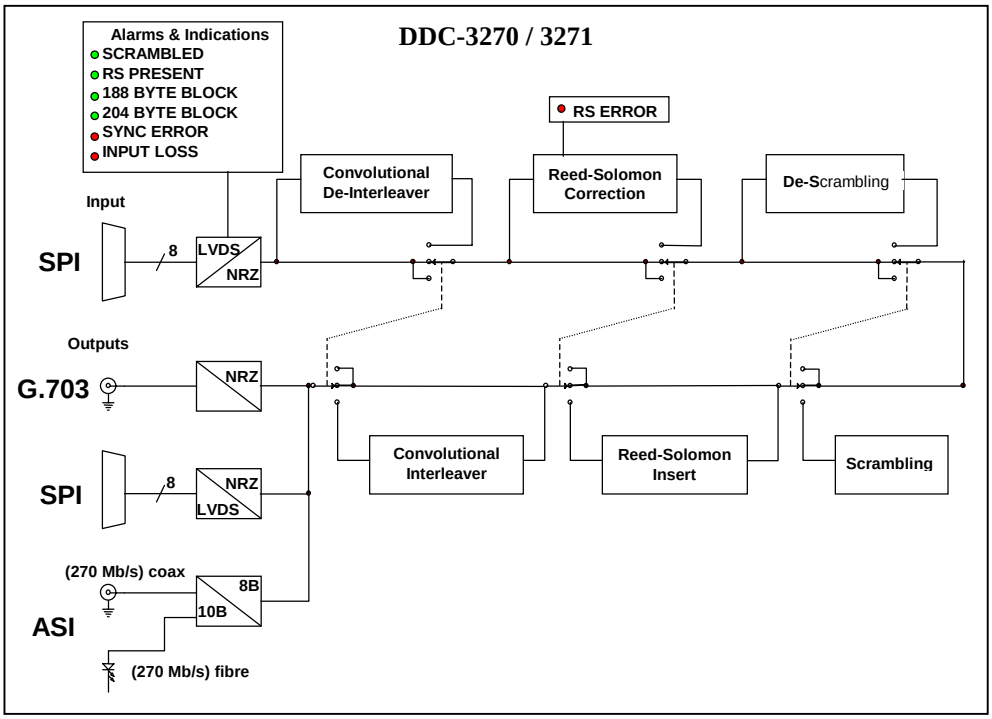
The QAM modulator is followed by interfacing to the Radio Frequency (RF) cable channel.

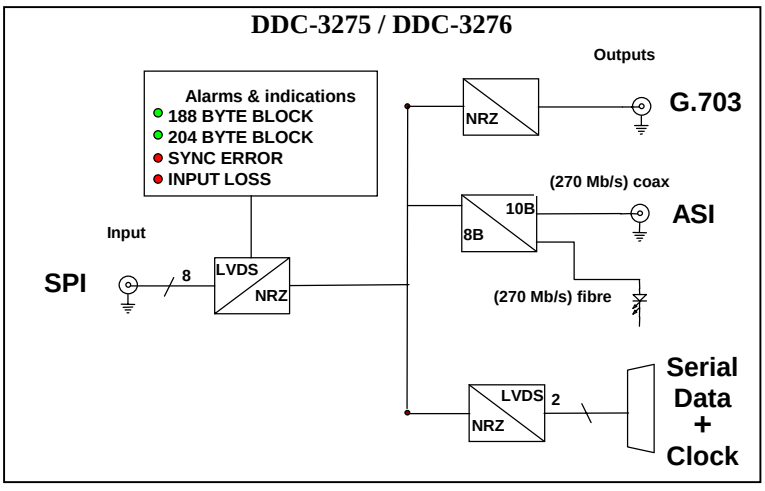
Cable receiver

A System receiver performs the inverse signal processing, as described for the modulation process above, in order to recover the baseband signal.

Block diagrams







DDC-3260/3261 Technical Specifications

(Preliminary)

Input:

Type	1 x	Unframed G.703 HDB3 @ 34 Mb/s (DDC-3260).
	1 x	Unframed G.703 B3ZS @ 45 Mb/s (DDC-3261).
Connector		1.6/5.6 or BNC options.

Outputs: (Simultaneous)

Type	1 x	Reclocked unframed G.703 HDB3 (DDC-3260)
	1 x	Reclocked unframed G.703 B3ZS (DDC-3261), * Data rate out = data rate of G.703 input. 1.6/5.6 or BNC connector options.
	1 x	SPI 25 pin 'D' female connector.
	1 x	Serial Data + Clock 15 pin 'D' male connector.
	1 x	ASI-C 75Ω, 800 mVp-p, BNC connector.
	1 x	ASI-O 1300 nm LED, 62.5/125 µm multimode fibre, launch power between -14 & -20 dBm SC connector.

* DDC-3261 may be set by on board link for shaped or unshaped G.703 output.

Alarms:

General alarm	Sync error / input loss/ power loss. 1 set N/O & 1 set N/C contacts, 4 pin 0.1" IDC male connector.
Power Requirements	28 Vac CT (14-0-14) or ± 16 Vdc.
Power consumption	<7 VA.

Other:

Temperature range		0 - 50° C ambient.
Mechanical		Suitable for mounting in IRT 19" rack chassis with input, output and power connections on the rear panel.
Finish:	Front panel	Grey enamel, silk-screened black lettering & red IRT logo.
	Rear assembly	Detachable silk-screened PCB with direct mount connectors to Eurocard and external signals.
Dimensions		6 HP x 3 U x 220 mm IRT Eurocard.
Supplied accessories		Rear connector assembly including matching connector for alarm output.

DC-3270/3271 Technical Specifications

(Preliminary)

Input:

Type		1 x SPI, 25 pin 'D' female connector. Data rate 22 to 48 Mb/s.

Outputs: (Simultaneous)

Type	1 x	Reclocked unframed G.703 HDB3 (DDC-3270)
	1 x	Reclocked unframed G.703 B3ZS (DDC-3271), Data rate out = data rate of SPI input. 1.6/5.6 or BNC connector options.
	1 x	SPI 25 pin 'D' female connector.
	1 x	ASI-C 75Ω, 800 mVp-p, BNC connector.
	1 x	ASI-O 1300 nm LED, 62.5/125 µm multimode fibre, launch power between -14 & -20 dBm. SC connector.

Alarm:

General alarm	Sync error / input loss/ power loss. 1 set N/O or 1 set N/C contacts, set by on board link. 2 pin 0.1" IDC male connector.
Power Requirements	28 Vac CT (14-0-14) or ± 16 Vdc.
Power consumption	<8 VA.

Other:

Temperature range		0 - 50° C ambient
Mechanical		Suitable for mounting in IRT 19" rack chassis with input, output and power connections on the rear panel.
Finish:	Front panel	Grey enamel, silk-screened black lettering & red IRT logo.
	Rear assembly	Detachable silk-screened PCB with direct mount connectors to Eurocard and external signals.
Dimensions		6 HP x 3 U x 220 mm IRT Eurocard.
Supplied accessories		Rear connector assembly including matching connector for alarm output.

DDC-3275/3276 Technical Specifications

(Preliminary)

Input:

Type	1 x	SPI Data rate 22 to 48 Mb/s. 25 pin 'D' female connector.

Outputs: (Simultaneous)

Type	1 x	Reclocked unframed G.703 HDB3 (DDC-3275)
	1 x	Reclocked unframed G.703 B3ZS (DDC-3276), Data rate out = data rate of SPI input. 1.6/5.6 or BNC connector options.
	1 x	Serial Data + Clock, 15 pin 'D' male connector.
	1 x	ASI-C 75Ω, 800 mVp-p, BNC connector.
	1 x	ASI-O 1300 nm LED, 62.5/125 μm multimode fibre, launch power between -14 & -20 dBm, SC connector.

Alarm:

General alarm	Sync error / input loss/ power loss. 1 set N/O or 1 set N/C contacts, set by on board link. 2 pin 0.1" IDC male connector.
Power Requirements	28 Vac CT (14-0-14) or ± 16 Vdc.
Power consumption	<5 VA.

Other:

Temperature range		0 - 50° C ambient
Mechanical		Suitable for mounting in IRT 19" rack chassis with input, output and power connections on the rear panel.
Finish:	Front panel	Grey enamel, silk-screened black lettering & red IRT logo.
	Rear assembly	Detachable silk-screened PCB with direct mount connectors to Eurocard and external signals.
Dimensions		6 HP x 3 U x 220 mm IRT Eurocard.
Supplied accessories		Rear connector assembly including matching connector for alarm output.

Due to our policy of continuing development, these specifications are subject to change without notice.

Converts 34 Mbit/s unframed G.703 (45 Mbit/s DDC-3261) into SPI, ASI (cable and optical), Serial Data + Clock and reclocked 34 Mbit/s (45 Mbit/s DDC-3261) unframed G.703. This module does not perform any processing (e.g. RS coding, interleaving energy dispersion correction etc) but rather de-serialises and decodes the G.703 input and detects MPEG TS sync errors.

G.703 Input
The input section used in DDC-3260 & DDC-3261 is similar to that used in the DDA-3100 (34 Mbit/s) & DDA-3300 (45 Mbit/s) data distribution amplifiers.
The signal from the rear panel connector passes to the input transformer and automatic line equalisation circuit. The purpose of this equaliser is to restore both the signal level and the leading and trailing edges of the digital signal so that signal jitter is reduced prior to the clock signal being derived in the subsequent stage.

+ve & -ve mark signals and clock generator.
The equalised signal is coupled to the following stages by transformer. This has two secondary windings to translate the positive and negative going components of the signal to a positive format for processing by standard single supply logic circuits in the following stages. The two signals are identified as the +ve and -ve mark signals and remain separate until the final output driver stage.

A synchronous clock signal is required by both the logic and reclocking circuits. The clock is an oscillator, which is re-triggered to keep time by a signal extracted from both the +ve or -ve mark signals.
The clock signal is retarded by delay line prior to being used in the main processing logic and reclocking circuit in order to provide the optimum timing at the reclocking point.

Logic processing, reclocking and error detection.
The reclocked G.703 output does not pass through the FPGA,
A dedicated CPLD is used to de-serialise the data before the FPGA. The FPGA runs at parallel data rate thus lowering the FPGA maximum processing rate.

The main logic processing, reclocking, error detection and operational interfacing are all performed by logic circuits within a custom programmed large scale logic array. The internal logic and functions of this IC are too complex to describe in detail and the following is intended as a guide to function only.

Data loss detection.
More than 255 x 8 consecutive 1's or 0's is deemed as a loss of Input. This number was selected to give a safe margin over the maximum length between TS syncs of 204 Bytes. A valid input must be applied for approximately 300 ms before the alarm is reset.

Input TS Sync Error
After 2 consecutive TS syncs are missed a TS Sync Error is deemed to have occurred. The Sync error is reset only after 5 consecutive TS syncs have been detected. The SYNC Error LED lights when a Sync error has been detected and remains lit for approximately 300 ms after the Sync error has been reset.

188 TS Sync length indicator
If the number of bytes between TS syncs is 188 then the 188 LED lights. When either a loss of input or sync loss is detected, this LED is extinguished.

204 TS Sync length indicator
If the number of bytes between TS syncs is 204 then the 204 LED lights. When either a loss of input or sync loss is detected, this LED is extinguished.

Alarm relay
Alarm outputs are available on the rear assembly using the J2 connector. Separate N/O & N/C are provided.
The relay is triggered upon loss of input or sync error. The N/O contact is to be preferred as it switches upon loss of power or removal of the DDC-3260 (DDC-3261) from its rear assembly.

Power on reset.
A power on reset signal is generated when power is applied to the unit. This signal causes the processing circuit to examine its current status and connections and restore operation.

SPI Output
The SPI output uses differential LVDS signalling with a standard 25 pin 'D' female connector.
The output is disabled when the Input Loss Alarm is triggered. See DDC-3260 *Configuration*.

ASI Output
ASI operates at 270 Mbit/s and uses 8B/10B coding with K28.5 stuffing bytes. The DDC-3260 implements the data burst method of K28.5 stuffing. The ASI cable output uses a 75 Ohm BNC connector whilst the ASI optical output uses a 1300 nm LED with SC connector. The LED output power level is approximately -16 dBm. A DVR-3210 optical receiver can be used to convert the optical signal back to ASI Cable (Non inverting outputs only).

Serial Data + Clock Output
The Serial Data + Clock interface transmits Serial Clock and Serial Data using LVDS logic levels and a standard 15 pin 'D' male connector.
The output is disabled when the Input Loss Alarm is triggered..

G.703 Output
HDB3 decoding (B3ZS DDC-3261) and G.703 output driving is performed by the EXAR XR-T7296 Integrated Line Transmitter. The G.703 output is a direct reflection of the G.703 input except when a Loss of Input is encountered. Therefore, any 34.368 Mbit/s HDB3 (44.736 Mbit/s B3ZS DDC-3261) input will be passed as long as the Loss of Input alarm is not triggered. (See *Input Loss Alarm*).

DDC-3270 & DDC-3271

The DDC-3270 processes an SPI input and outputs processed SPI, ASI (cable and optical) and 34 Mbit/s Unframed G.703 (45 Mbit/s DDC-3271). This module is capable of performing scrambling, de-scrambling, RS encoding, RS decoding, interleaving and de-interleaving. It can encode as well as decode different MPEG TS formats. The module is normally set up as either a decoder or an encoder. Combinations of both functions simultaneously are somewhat difficult and should be avoided.

The processing functions are selected using three switches (interleaving, RS coding and scrambling) on the front panel. Each switch has three positions (up, centre or down).
The DDC-3270 is internally divided into a decoder followed by an encoder.
A switch set to the UP position applies processing to the decoding section; a switch set to the DOWN position applies processing to the encoding section; and a switch set to the CENTRE position does not perform that function to either the decoding or encoding section.
Applying a function to both the decoder and encoder section simultaneously is prevented by means of each switch having only three positions. Full encoding and decoding is possible by using two DDC-3270 modules connected together, if this is ever required.

In most instances the DDC-3270 would be set to decoder mode with the de-interleaver and RS decoder functions enabled.

To generate a FOXTEL compliant TS stream from a Rohde & Schwarz DVG, the DDC-3270 would be set with the interleaver and RS encoder enabled.

SPI Output
The SPI output uses differential LVDS signalling with a standard 25 pin 'D' female connector.
The output is disabled when Input Loss Alarm is triggered.

ASI Output
ASI operates at 270 Mbit/s and uses 8B/10B coding with K28.5 stuffing bytes. The DDC-3270 (DDC-3271) implements the data burst method of K28.5 stuffing. The ASI cable output uses a 75 Ohm BNC whilst the ASI optical output uses a 1300 nm LED. The LED output power level is approximately -17.0 dBm. A DVR-3210 optical receiver can be used to convert the optical signal back to ASI Cable (Non inverting outputs only).

G.703 Output
The G.703 output is the processed TS format. The G.703 output is disabled during loss of SPI input.

Input Loss Alarms
The Input Loss Alarm will be asserted in the absence of SPI input clock.

Input TS Sync Error
After 2 consecutive TS syncs are missed a TS Sync Error is deemed to have occurred. The Sync error is reset only after 5 consecutive TS syncs have been detected. The SYNC Error LED lights when a Sync error has been detected and remains lit for approximately 300 ms after the Sync error has been reset.

188 TS Sync length indicator
If the number of bytes between TS syncs is 188 then the 188 LED lights.

204 TS Sync length indicator
If the number of bytes between TS syncs is 204 then the 204 LED lights.

Alarm relay
Alarm outputs are available on the rear assembly using the J 2 connector. N/O & N/C outputs can be selected using LK 1. The relay is triggered upon loss of input or sync error. The N/O contact is preferred as it switches upon loss of power or removal of the DDC-3270 (DDC-3271) from its rear assembly.

LED indicators 188 TS Byte length, 204 TS Byte length, CRC error, Scram present, RS present are blanked during Input loss or sync loss.

DDC-3275 & DDC-3276

The DDC-3275 (DDC-3276) converts SPI to 34 Mbit/s G703, ASI (cable and optical) and Serial Data + Clock. This module does not perform any processing (e.g. RS coding, interleaving scrambling etc) but rather serialises the SPI input detects MPEG TS sync. This module is the complement to the DDC-3260 (DDC-3261).

In most cases the DDC-3275 is not required if a DDC-3270 (DDC-3271) is being used to process the signal. However, the DDC-3270 (DDC-3271) does not have a LVDS Data + Clock output, whereas the DDC-3275 (DDC-3276) does. In other cases where processing is not required, the DDC-3275 (DDC-3276) provides a cost effective alternative to the DDC-3270 (DDC-3271) and eliminates the possibility of inadvertent coding selections being made.

The internal circuitry of the DDC-3275 (DDC-3276) is similar to that of the DDC-3270 (DDC-3276) previously described, without the coding options.

SPI Output
The SPI output uses differential LVDS signalling with a standard 25 pin 'D' female connector.
The output is disabled when Input Loss Alarm is triggered.

ASI Output
ASI operates at 270 Mbit/s and uses 8B/10B coding with K28.5 stuffing bytes. The DDC-3275 (DDC-3276) implements the data burst method of K28.5 stuffing. The ASI cable output uses a 75 Ohm BNC whilst the ASI optical output uses a 1300 nm LED. The LED output power level is approximately -17.0 dBm. A DVR-3210 optical receiver can be used to convert the optical signal back to ASI Cable (Non inverting outputs only).

Serial Data + Clock Output
The Serial Data + Clock interface transmits Serial Clock and Serial Data using LVDS logic levels and a standard 15 pin 'D' male connector.

G.703 Output
The G.703 output is the processed TS format. The G.703 output is disabled during loss of SPI input.

Input Loss Alarms
The Input Loss Alarm will be asserted in the absence of SPI input clock.

Input TS Sync Error
After 2 consecutive TS syncs are missed a TS Sync Error is deemed to have occurred. The Sync error is reset only after 5 consecutive TS syncs have been detected. The SYNC Error LED lights when a Sync error has been detected and remains lit for approximately 300 ms after the Sync error has been reset.

188 TS Sync length indicator
If the number of bytes between TS syncs is 188 then the 188 LED lights.

204 TS Sync length indicator
If the number of bytes between TS syncs is 204 then the 204 LED lights.

Alarm relay
Alarm outputs are available on the rear assembly using the J 2 connector. N/O & N/C outputs can be selected using LK 6. The relay is triggered upon loss of input or sync error. The N/O contact is preferred as it switches upon loss of power or removal of the DDC-3275 (DDC-3276) from its rear assembly.

Internal adjustments

The following adjustable resistors are factory set. They should not be adjusted by the user. The following information is included for general information purposes only. Any adjustment of these controls without factory test facilities is likely to render inoperable the corresponding section of the module.

DDC-3260/3261: RV 1 ASI-O linearity.
RV 3 G.703 clock recovery bias.

DDC-3270/3271: RV 1 ASI-O linearity.

DDC-3275/3276: RV 1 ASI-O linearity.

Configuration

Links & options:

Warning:
Some of the following links are for factory use only during set-up and should not be changed.
Links may be changed without disconnecting power. However, when any link is changed, normal decoding of the MPEG TS will be disturbed. The time taken before normal decoding resumes is dependent on the decoder in use and may be up to five seconds.

DDC-3260 & DDC-3261

LK 1: XXX Factory set delay line setting - do not change.

LK 2: XXX Factory set delay line setting - do not change.

LK 3: OUT Reserved

LK 4: OUT Reserved

LK 5: OUT Reserved

LK 6: OUT Factory set - DDC-3260.
IN Factory set - DDC-3261.

LK 7: OUT Supports both 204 & 188 byte MPEG-2 TS formats. (Normal position)
IN Supports only 204 byte MPEG-2 TS formats. (This position is only intended for use in high BER situations to lower the possibility of false lock.)

LK 8: OUT Passes RS data (if present) as received. (normal position when used in conjunction with DDC-3270/DDC-3271)
IN Replace RS data bytes with dummy bytes and de-asserts DVALID output.

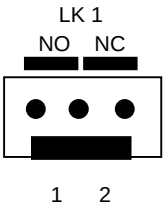
LK 9: OUT Does not disable SPI output upon input loss.
IN Disables SPI output upon input loss.

DDC-3260 Foxtel / Telstra initial setup:

LK 1 XXX Factory set delay line setting - do not change
LK 2 XXX Factory set delay line setting - do not change
LK 3 OUT
LK 4 OUT
LK 5 OUT
LK 6 OUT
LK 7 OUT
LK 8 OUT
LK 9 IN

DDC-3270 & DDC-3271

LK 1: J 2 Alarm relay output



LK 2: OUT Passes RS data (if present) as received. (Normal position when used in conjunction with DDC-3260.)
IN Replace RS data bytes with dummy bytes and de-asserts DVALID output.

LK 3: OUT Reserved

LK 4: IN Reserved

LK 5: OUT Reserved

DDC-3270 Foxtel / Telstra initial setup:

LK 2 IN
LK 3 OUT
LK 4 IN
LK 5 OUT

DDC-3275 & DDC-3276

LK 1: OUT Reserved

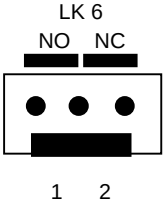
LK 2: OUT Reserved

LK 3: OUT Reserved

LK 4: OUT Reserved

LK 5: OUT Reserved

LK 6: J 2 Alarm relay output



Operational Safety

WARNING

Operation of electronic equipment involves the use of voltages and currents that may be dangerous to human life. Note that under certain conditions dangerous potentials may exist in some circuits when power controls are in the **OFF** position. Maintenance personnel should observe all safety regulations.

Do not make any adjustments inside equipment with power **ON** unless proper precautions are observed. All internal adjustments should only be made by suitably qualified personnel. All operational adjustments are available externally without the need for removing covers or use of extender cards.

Pre-Installation:

Handling:

This equipment may contain or be connected to static sensitive devices and proper static free handling precautions should be observed.

Where individual circuit cards are stored, they should be placed in antistatic bags and proper antistatic procedures should be followed when inserting or removing cards from these bags.

Power:

AC mains supply: Ensure that operating voltage of unit and local supply voltage match and that correct rating fuse is installed for local supply.

DC supply: Ensure that the correct polarity is observed and that DC supply voltage is maintained within the operating range specified.

Earthing:

The earth path is dependent on the type of frame selected. In every case particular care should be taken to ensure that the frame is connected to earth for safety reasons. See frame manual for details.

Signal earth: For safety reasons a connection is made between signal earth and chassis earth. No attempt should be made to break this connection.

Installation in frame or chassis:

See details in separate manual for selected frame type.

Connections:

SPI connectors:
The SPI uses 25 pin 'D' connectors. Cable connectors are male and equipment connectors are female. Interconnecting cables and connectors must be shielded. Logic levels are LVDS.

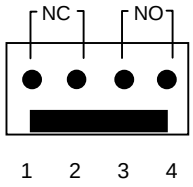
Pin	Signal line	Pin	Signal line
l	Clock A	14	Clock B
2	System Gnd	15	System Gnd
3	Data 7 A(MSB)	16	Data 7 B
4	Data 6 A	17	Data 6 B
5	Data 5 A	18	Data 5 B
6	Data 4 A	19	Data 4 B
7	Data 3 A	20	Data 3 B
8	Data 2 A	21	Data 2 B
9	Data l A	22	Data 1 B
10	Data 0 A	23	Data 0 B
11	DVALID A	24	DVALID B
12	PSYNC A	25	PSYNC B
13	Cable Shield		

Serial Data + Clock output:
The Serial Data + Clock uses 15 pin 'D' connectors. Cable connectors are female and equipment connectors are male. Interconnecting cables and connectors must be shielded. Logic levels are LVDS.

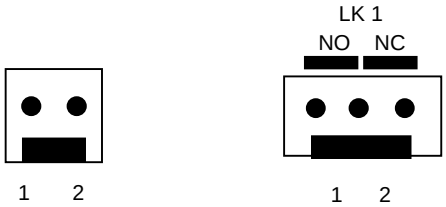
Pin	Signal	Pin	Signal
1	Protective Gnd	9	Data -
2	Data +	10	
3		11	
4		12	
5		13	
6		14	Clock -
7	Clock +	15	
8	Signal Gnd		

Alarm connections:

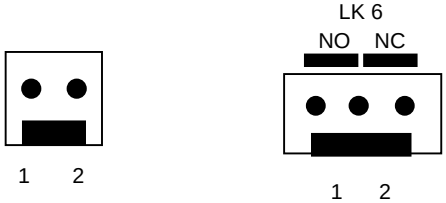
DDC-3260/3261
J 2 Alarm relay output



DDC-3270/3271
J 2 Alarm relay output

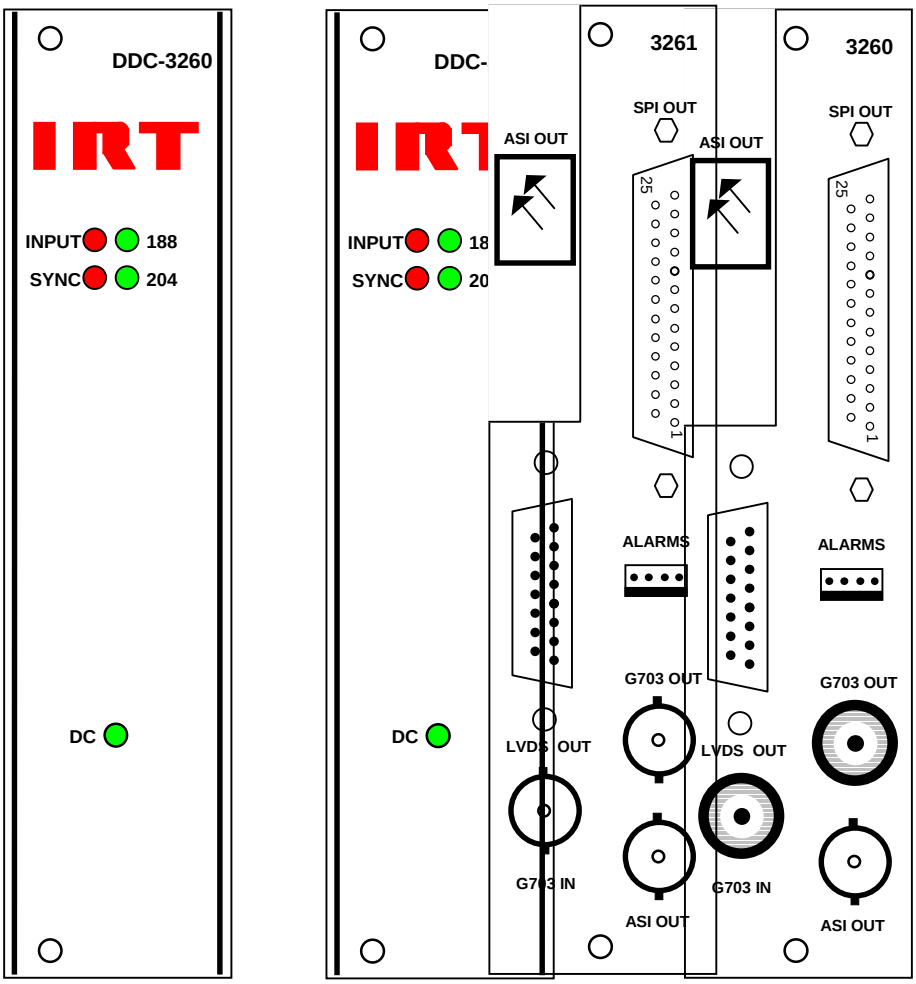


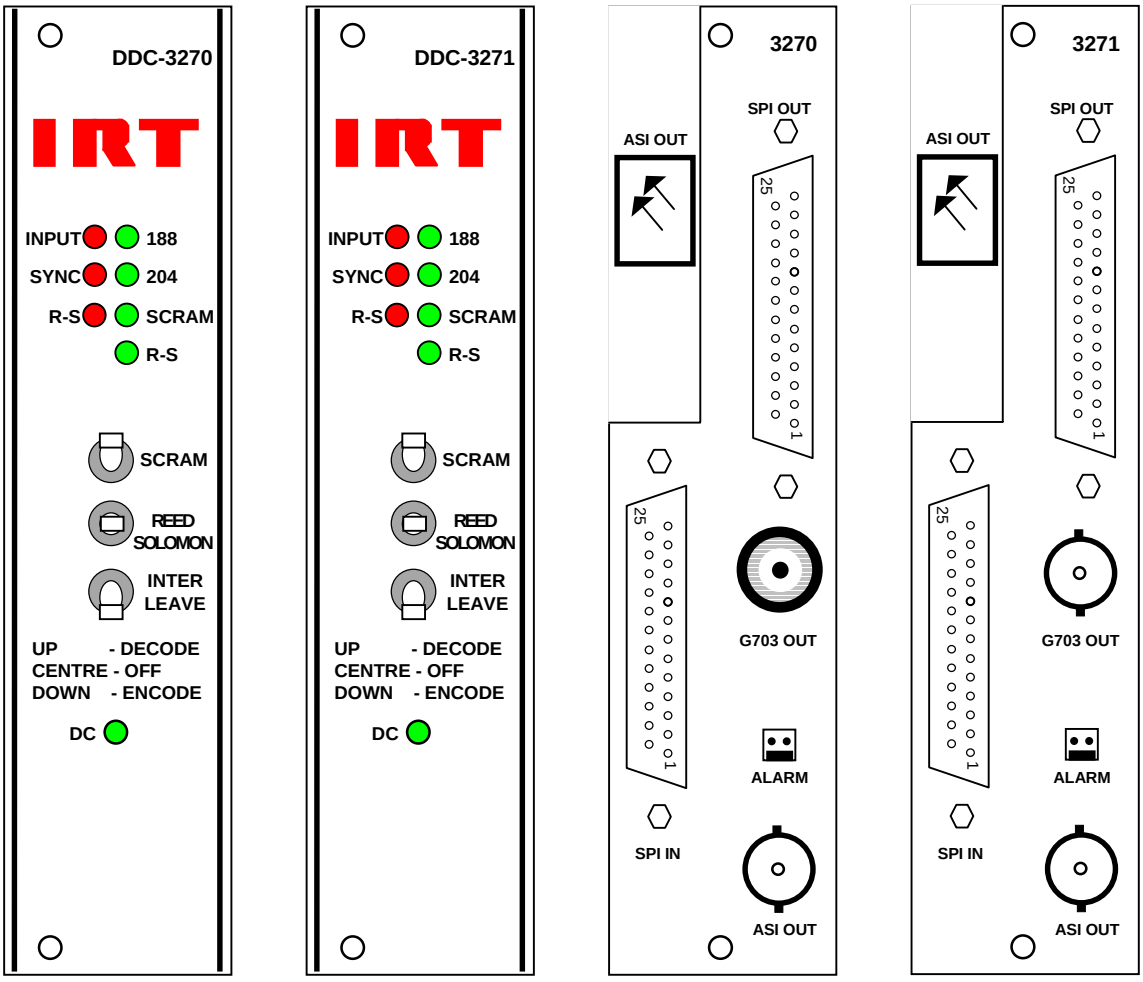
DDC-3275/3276
J 2 Alarm relay output

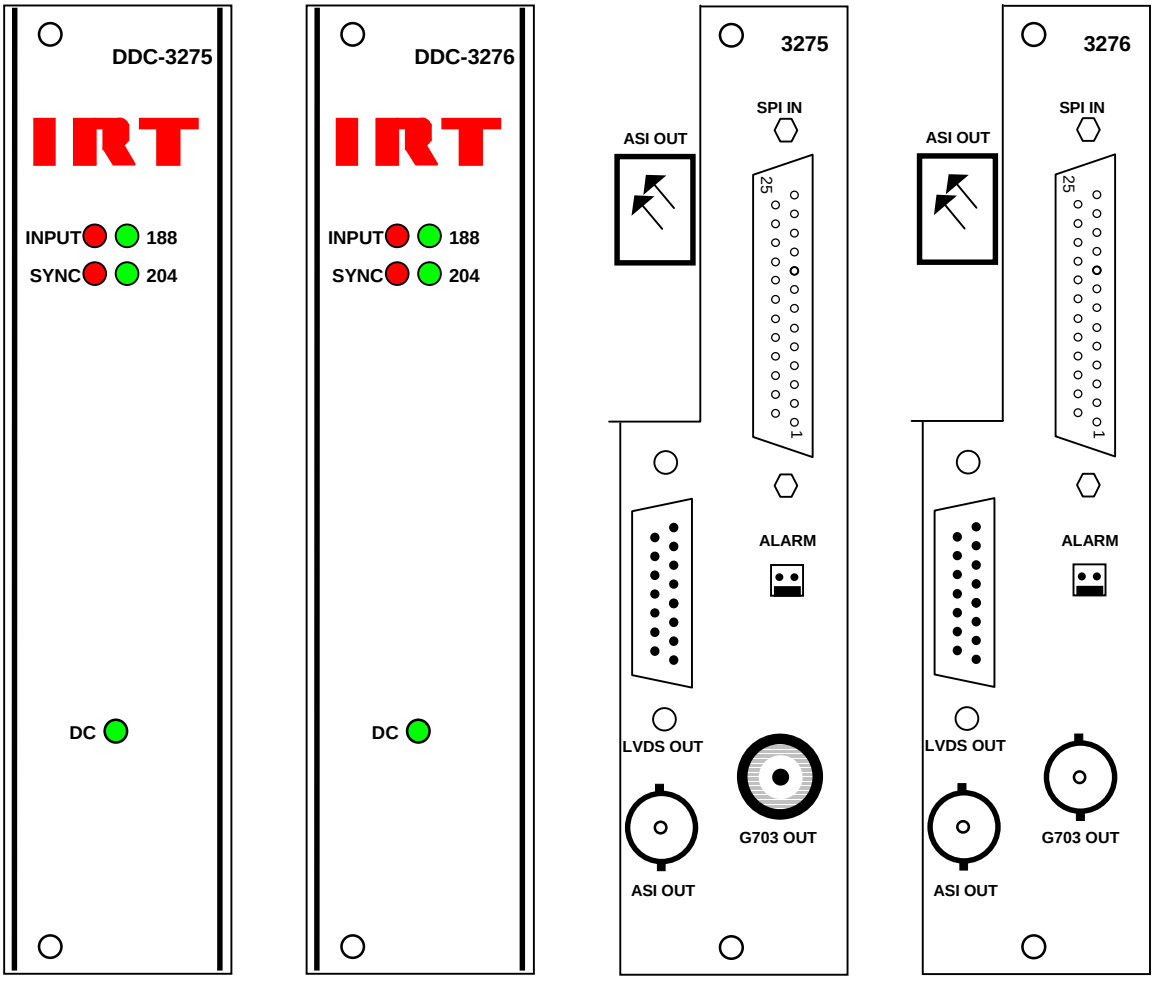


Front & rear panel connector diagrams

The following front panel and rear assembly drawings are not to scale and are intended to show relative positions of connectors, indicators and controls only.



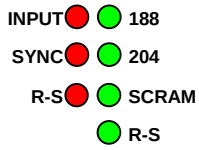

DDC-3270
IRT
INPUT
188
SYNC
204
R-S
SCRAM
R-S
SCRAM
REED SOLOMON
INTER LEAVE
UP - DECODE
CENTRE - OFF
DOWN - ENCODE
DC
DDC-3271
IRT
INPUT
188
SYNC
204
R-S
SCRAM
R-S
SCRAM
REED SOLOMON
INTER LEAVE
UP - DECODE
CENTRE - OFF
DOWN - ENCODE
DC
3270
ASI OUT
SPI OUT
25
1
G703 OUT
ALARM
SPI IN
ASI OUT
3271
ASI OUT
SPI OUT
25
1
G703 OUT
ALARM
SPI IN
ASI OUT


DDC-3275
IRT
INPUT
188
SYNC
204
DC
DDC-3276
IRT
INPUT
188
SYNC
204
DC
3275
ASI OUT
SPI IN
25
1
ALARM
LVDS OUT
G703 OUT
ASI OUT
3276
ASI OUT
SPI IN
25
1
ALARM
LVDS OUT
G703 OUT
ASI OUT

Operation

Front indicators:

Input loss alarm:
This LED lights when no data transmission is detected at the input for a given time. MPEG-2 TS always contain a sync byte every 204 or 188 bytes irrespective of data content. Therefore, if 2040 or more, consecutive 1's or 0's are been detected; then the input is deemed lost.



Sync loss alarm:
This LED lights for at least 300 ms when two or more MPEG-2 TS sync bytes are absent. The LED extinguishes when five or more correct SYNC bytes are detected.

188 byte indicator:
This LED lights when a valid MPEG-2 TS stream containing 188 bytes between sync bytes is detected.

204 byte indicator:
This LED lights when a valid MPEG-2 TS stream containing 204 bytes between sync bytes is detected.

Scrambling presence indicator: (DDC-3270 & DDC-3271 only.)
This LED lights when a valid MPEG-2 TS stream containing a byte sequence that corresponds to scrambling. A scrambling byte sequence uses an inverted 47H sync byte (B8H) every eighth sync to signify the start of the scrambling sequence.

RS (Reed Solomon) presence indicator: (DDC-3270 & DDC-3271 only.)
This LED lights when Reed Solomon error correction bytes are present in place of the 16 dummy bytes of a 204 Byte MPEG-2 TS. The DDC-3270 considers any data content other than all 0's during the 16 dummy bytes to be RS correction bytes.

DDC-3270 & DDC-3271 processing controls:

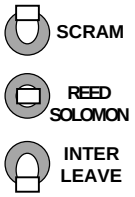
This module is capable of performing scrambling, de-scrambling, RS encoding, RS decoding, interleaving and de-interleaving. It can encode or decode different MPEG TS formats.

In this context, the word scrambling refers to the process of Sync1 inversion and randomisation for the purpose of energy dispersal of the signal. It does not refer to the encryption applied to Pay TV signals to control access to particular channels or programs.

For a description of the processes involved see *Application examples - Cable Systems* and *Technical specifications - Characteristics of signal types - MPEG-2 transport layer coding*.

The module is normally set up as either a decoder or an encoder. Combinations of both functions simultaneously should be avoided.

The processing functions are selected using three switches (interleaving, RS coding and scrambling) on the front panel. Each switch has three positions (up, centre or down).



UP - DECODE
CENTRE - OFF
DOWN - ENCODE

The DDC-3270 is internally divided into a decoder followed by an encoder. See *Block diagrams*.

A switch set to the UP position applies processing to the decoding section;
a switch set to the DOWN position applies processing to the encoding section;
and a switch set to the CENTRE position does not perform that function to either the decoding or encoding section.

Applying a function to both the decoder and encoder section simultaneously is prevented by means of each switch having only three positions. Full encoding and decoding is possible by using two DDC-3270 modules connected together, if this is ever required.

In most instances, the DDC-3270 would be set to decoder mode with the de-interleaver and RS decoder functions enabled.
See *Application examples* for further information.

DDC-3270 Foxtel / Telstra initial setup:

DDC-3270 only.	
SCRAM switch	Centre
Reed-Solomon switch	UP
Interleave	UP

Maintenance & Storage

Maintenance:

No regular maintenance is required.

Care however should be taken to ensure that all connectors are kept clean and free from contamination of any kind. This is especially important in fibre optic equipment where cleanliness of optical connections is critical to performance.

Storage:

If the equipment is not to be used for an extended period it is recommended the whole unit be placed in a sealed plastic bag to prevent dust contamination. In areas of high humidity a suitably sized bag of silica gel should be included to assist deter corrosion.

Where individual circuit cards are stored, they should be placed in antistatic bags and proper antistatic procedures should be followed when inserting or removing cards from these bags.

Warranty & Service

Equipment is covered by a limited warranty period of five years within Australia (3 years International) from date of first delivery unless contrary conditions apply under a particular contract of supply.

Equipment warranty is limited to faults attributable to defects in original design or manufacture. Warranty on components shall be extended by IRT only to the extent obtainable from the component supplier.

Equipment return:

Prior to arranging service ensure that the fault is in the unit to be serviced and not in associated equipment. If possible confirm this by substitution.

Before returning equipment contact should be made with IRT or your local agent to determine whether the equipment can be serviced in the field or should be returned for repair.

The equipment should be properly packed for return observing antistatic procedures.

The following information should accompany the unit to be returned:

1. A fault report should be included indicating the nature of the fault
2. The operating conditions under which the fault initially occurred.
3. Any additional information which may be of assistance in fault location and remedy.
4. A contact name and phone and fax numbers.
5. Details of payment method for items not covered by warranty.
6. Full return address.

Please note that all freight charges are the responsibility of the customer.

The equipment should be returned **to the agent who originally supplied the equipment or, where this is not possible**, to IRT direct as follows.

Equipment Service
IRT Electronics Pty Ltd
26 Hotham Parade
ARTARMON
N.S.W. 2064
AUSTRALIA

Phone: 61 2 9439 3744
Fax: 61 2 9439 7439

Characteristics of signal types

Coding characteristics

G.703:

The **HDB3** (High Density Bi-polar of order 3) code as defined in G.703 for 34,368 Kbits/s is as follows:

Binary 1 bits are represented by alternate positive and negative pulses and binary 0 bits by spaces. Exceptions are made when strings of successive 0 bits occur in the binary signal.

Each block of 4 successive zeros is replaced by 000V or B00V where B is an inserted pulse of the correct polarity and V is an inserted pulse violating the polarity rule. The choice of 000V or B00V is made so that the number of B pulses between consecutive V pulses is odd so that successive V pulses are of alternate polarity and so no DC component is introduced.

The **B3ZS** (Bipolar with Three Zero Substitution) (Also designated **HDB2** - High Density Bi-polar of order 2) code as defined in G.703 for 44,736 Kbits/s is as follows:

Binary 1 bits are represented by alternate positive and negative pulses and binary 0 bits by spaces. Exceptions are made when strings of successive 0 bits occur in the binary signal.

Each block of 3 successive zeros is replaced by 00V or B0V. The choice of 00V or B0V is made so that the number of B pulses between consecutive V pulses is odd, so that successive V pulses are of alternate polarity and so no DC component is introduced.

Synchronous Parallel Interface (SPI)

SPI is a system for parallel transmission of variable data rates. The data transfer is synchronised to the Byte clock of the MPEG transport stream.

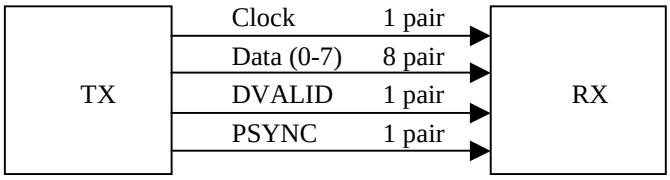
The data to be transmitted are MPEG-2 transport packets. The data signals are synchronised to the clock depending on the transmission rate.

The parallel interface has three allowable transmission formats:

188 byte packets
204 Byte packets (188 data Bytes + 16 dummy Bytes)
204 byte packets (188 data Bytes + 16 additional valid Bytes)

The clock, data and synchronisation signals are transmitted in parallel. They comprise 8 data bits together with one (MPEG-2) PSYNC signal and a DVALID signal.
The DVALID signal indicates in the 204 Byte mode that the additional space is filled with dummy Bytes.
All signals are synchronous to the clock signal. The signals are coded in NRZ form.

The clock is a square wave signal where the 0-1 transition represents the data transfer time. The clock frequency depends on the transmission rate. The frequency corresponds to the useful bitrate of the MPEG2 transport layer and shall not exceed 13.5 MHz.



= 11 pair in total.

Electrical characteristics of the interface
Each of the eleven line drivers (source) has a balanced output and each line receiver (destination) a balanced input employing LVDS drivers / receivers. All digital signal time intervals are measured between the half-amplitude points.

Logic convention
A binary 1 is represented by the non-inverted output being positive with respect to the inverted output.
A binary 0 is represented by the non-inverted output being negative with respect to the inverted output.

Asynchronous Serial Interface (ASI)

The Asynchronous Serial Interface (ASI) provides a system for serial encoded transmission of different data rates with a constant transmission rate of 270 Mbit/s.
The ASI standard supports coaxial cable and multi-mode fibre-optic cable (using LED emitters).

ASI Protocol Architecture Description

The ASI protocol is divided into three architectural layers: Layer-0, Layer-1 and Layer-2.
MPEG Transport Packets form the top layer (Layer 2), and the bottom layers are based upon the Fibre Channel Standard (Layers 1 and 0). Layer 2 is defined using the MPEG-2 Standard ISO/IEC 13818-1 (Systems). Layers 1 and 0 are based upon a subset of ANSI Standard X3T11/ Levels FC-1 and FC-0.

Layer-O: Physical Requirements

The physical Layer defines the transmission media, the drivers and receivers, and the transmission speeds. The physical interface provides for both LED-driven multimode fibre and copper coaxial cable.

Line Rates and Bit Timing

The encoded line rate with the 8B/10B block code is 270 Mbit/s which results in a media transmission rate of 270 MBaud. At the transmitter, the serialisation is done using a fixed oscillator to establish this 270 MBaud rate from which a phase-locked Byte clock is derived and used to shift in parallel Bytes.

Receivers recover the serial transmission clock. A phase-locked Byte clock is derived from this recovered serial bit clock and is used to shift parallel Bytes out to Layer- 1 processing elements. It is required that the encoded line rate shall be 270 MBaud ±100 ppm.

Layer-1 Data Encoding

The ASI Transmission Layer 1 deals with encoding/decoding aspects, which are independent of the transmission medium characteristics. The encoding method utilised is specified in the fibre channel document X3T11

At Layer-1, Bytes are 8B/10B coded, which produces one 10-bit word for each 8-bit Byte presented.
The 8B/10B transmission coding provides for both a self checking capability and Byte synchronisation of the link. The 10B transmission code is defined in terms of "disparity": the difference in the number of "1" bits and "0" bits in the transmitted serial data stream. The disparity characteristics of the code maintain DC balance.
Special characters are defined as extra code points beyond the need to encode a Byte of data. One in particular is used to establish Byte synchronisation in the ASI transmission link.

The 10-bit words are then passed through a parallel-to-serial converter, which operates at a fixed output bit-rate of 270 Mbit/s.. If the converter requests a new input word and the data source does not have one ready, a synchronisation word is inserted. These sync words are ignored by receive equipment.
The resulting serial bit stream is passed to the output driver circuit for coaxial or fibre-optic cable.

Receive data arriving on a coaxial cable or fibre is first coupled to a circuit, which recovers clock and data.
Recovered serial data bits are passed to a 10B/8B decoder that converts the 10-bit transmission words back into the 8-bit Bytes originally transmitted. In order to recover Byte alignment, the 10B/8B decoder initially searches for synchronisation words. Once found, the start of the synchronisation word marks the boundary of subsequent received data words and establishes proper Byte-alignment of decoder output Bytes.

NOTE - The ASI coding is sensitive to logical inversion of the transmitted bits. Therefore, to ensure correct operation, care must be taken that equipment interface circuitry of the non-inverting type is used.

The **Bit-Error-Rate (BER) Performance** shall be less than one part in 10^{13}.

Layer-2 Transport Protocol

The ASI Transmission Layer-2 standard uses the MPEG-2 Transport Stream Packet as defined in ISO/IEC 13818-1 (Systems) as its basic message unit. Optionally the RS coded Byte structure as specified in ETS 300 429 is also supported.

Data to be transmitted are presented in Byte-synchronised form as MPEG-2 Transport packets. Transport Packets may be presented to Layer-2 either as a burst of contiguous Bytes, or as individual Bytes spread out in time.

The ASI Interface Layer-2 definition employs the MPEG-2 Transport Stream packet syntax with the additional requirement that every Transport Packet shall be preceded with at least two synchronisation characters. This allows re-sync within one transport packet in the event that a line disturbance causes loss of sync.

MPEG-2 transport layer coding

The MPEG-2 Transport Layer is defined in ISO/IEC DIS 13818-1 [1]. The Transport Layer for MPEG-2 data is comprised of packets having 188 Bytes, with one Byte for synchronisation purposes, three Bytes of header containing service identification, scrambling and control information, followed by 184 Bytes of MPEG-2 or auxiliary data.
The framing organisation is based on the MPEG-2 transport packet structure.

Channel coding

To achieve the appropriate level of error protection required for cable transmission of digital data, a FEC based on Reed-Solomon encoding is used. In contrast to the Baseline System for satellite described in ETS 300 421, no convolutional coding is applied to cable transmission. Protection against burst errors is achieved by the use of Byte interleaving.

Randomisation for spectrum shaping (Scrambling)
The System input stream is organised in fixed length packets (see figure 2), following the MPEG-2 transport multiplexer. The total packet length of the MPEG-2 transport MUX packet is 188 Bytes. This includes 1 sync-word Byte (i.e. 47_{HEX}). The processing order at the transmitting side shall always start from the MSB (i.e. 0) of the sync word-Byte (i.e. 01000111).

In order to comply with the System for satellite, (see ETS 300 421) and to ensure adequate binary transitions for clock recovery, the data at the output of the MPEG-2 transport multiplex is randomised.

The polynomial for the Pseudo Random Binary Sequence (PRBS) generator is:

$1 + X^{14} + X^{15}$

Loading of the sequence 100101010000000" into the PRBS registers, is initiated at the start of every eight transport packets. To provide an initialisation signal for the de-scrambler, the MPEG-2 sync Byte of the first transport packet in a group of eight packets is bitwise inverted from 47_{HEX} to $B8_{HEX}$.

The first bit at the output of the PRBS generator is applied to the first bit of the first Byte following the inverted MPEG-2 sync Byte (i.e.$B8_{HEX}$). To aid other synchronisation functions, during the MPEG-2 sync Bytes of the subsequent 7 transport packets, the PRBS generation continues, but its output is disabled, leaving these Bytes unrandomised. The period of the PRBS sequence shall therefore be 1,503 Bytes.

The randomisation process is active also when the modulator input bit-stream is non-existent, or when it is non-compliant with the MPEG-2 transport stream format (i.e. 1 sync Byte + 187 packet Bytes). This is to avoid the emission of an unmodulated carrier from the modulator.

Reed-Solomon coding
Following the energy dispersal randomisation process, systematic shortened Reed-Solomon encoding is performed on each randomised MPEG-2 transport packet, with T = 8. This means that 8 erroneous Bytes per transport packet can be corrected. This process adds 16 parity Bytes to the MPEG-2 transport packet to give a codeword (204, 188).

NOTE: RS coding is applied also to the packet sync Byte, either non-inverted (i.e. 47_{HEX}) or inverted (i.e. $B8_{HEX}$).

Code Generator Polynomial: $g(x) = (x+\lambda^0)(x+\lambda^1)(x+\lambda^2) \ldots (x+\lambda^{15})$, where $\lambda = 02_{HEX}$

Field Generator Polynomial: $p(x) = x^8 + x^4 + x^3 + x^2 + 1$

The shortened Reed-Solomon code is implemented by appending 51 Bytes, all set to zero, before the information Bytes at the input of a (255, 239) encoder; after the coding procedure these Bytes are discarded.

Convolutional interleaving
Convolutional interleaving with depth I = 12 is applied to the error protected packets (see figure 2c). This results in an interleaved frame.

The convolutional interleaving process is based on the Forney approach which is compatible with the Ramsey type III approach, with I = 12. The Interleaved Frame is composed of overlapping error-protected packets and is delimited by MPEG-2 sync Bytes (preserving the periodicity of 204 Bytes).

The interleaver may be composed of I = 12 branches, cyclically connected to the input Byte-stream by the input switch. Each branch is a First In First Out (FIFO) shift register, with depth (Mj) cells (where M = 17 = N/I, N = 204 = error protected frame length, I = 12 = interleaving depth, = branch index). The cells of the FIFO shall contain 1 Byte, and the input and output switches is synchronised.

For synchronisation purposes, the sync Bytes and the inverted sync Bytes are always routed into the branch 0" of the interleaver (corresponding to a null delay).

The de-interleaver is similar, in principle, to the interleaver, but the branch indexes are reversed (i.e. j = 0 corresponds to the largest delay). The de-interleaver synchronisation can be carried out by routing the first recognised sync Byte into the "0" branch.

Electrical characteristics:

G.703 34 Mbit/s:

CCITT G.703 34368 Kb/s:

Cable type	Coaxial.
Impedance	75 Ω
Signal level	1.0 V
Nominal pulse width	14.55 ns
Code conversion	HDB3
Pulse shape	Fig. 17/G.703
Jitter at input port	§ 3 of recommendation G.823
Jitter at output port	§ 2 of recommendation G.823
Return loss at input ports:	
860 KHz to 1720 KHz	>12 dB
1720 KHz to 34368 KHz	>18 dB
34368 KHz to 51550 KHz	>14 dB

G.703 45 Mbit/s:

CCITT G.703 Shaped 44736 Kb/s:

Cable type	Coaxial.
Impedance	75 Ω
Signal level	
Power at 22368 KHz	+1.8 dBm to +5.7 dBm.
Power at 44736 KHz	>20 dBm below power at 22368 KHz.
Code conversion	B3ZS
Pulse shape	Fig. 14/G.703

Unshaped 44736 Kb/s:

Cable type	Coaxial.
Impedance	75 Ω
Signal level	1.0 V
Nominal pulse width	14.55 ns
Code conversion	B3ZS
Pulse shape	Fig. 17/G.703
Jitter at input port	§ 3 of recommendation G.823
Jitter at output port	§ 2 of recommendation G.823
Return loss at input ports:	
860 KHz to 1720 KHz	>12 dB
1720 KHz to 34368 KHz	>18 dB
34368 KHz to 51550 KHz	>14 dB

Electrical characteristics SPI:

Line Driver Characteristics (Source)

Output impedance	100 Ω maximum
Common mode voltage	1.125 V to 1.375 V
Signal amplitude	247 mV to 454 mV
Rise and fall times	< T/7, measured between the 20% and 80% amplitude points, with a 100 Ω resistive load. The difference between rise and fall times shall not exceed T/20.

Line Receiver Characteristics (Destination)

Input impedance	90 Ω to 132 Ω
Maximum input signal	2.0 Vp-p
Minimum input signal	100 mVp-p

Electrical characteristics ASI:

Transmitter output characteristics:

Output voltage	800 mVp-p ±10%.
Deterministic jitter	<10% p-p.
Random jitter	<8% p-p.
Rise/fall time (20-80%)	<1.2 ns.

Receiver input characteristics:

Minimum sensitivity (D21.5 idle pattern)	200 mV
Maximum input voltage	880 mVp-p
s_{11} (range: 0.1 to 1.0 x bit rate)	-17 dB
Minimum discrete connector return loss	15 dB (5 MHz - 270 MHz)

Fibre link:

Fibre core diameter 62.5 µm
Connector SC

Coaxial link:

Impedance 75 Ohm.
Equipment connector BNC female.

(Electrical measurements made with 75 Ohm resistive termination.)

Transmitter:

Type	LED
Spectral centre wavelength	1280 nm - 1380 nm
Launched power	-20 to -14 dBm
Extinction ratio	>9 dB.
Deterministic jitter	16 % p-p
Random jitter	9 % p-p
Optical rise time	<2.0 ns
Optical fall time	<2.2 ns

Receiver:

Received power	-26 to -14 dBm
Deterministic jitter	19 % p-p
Random jitter	9 % p-p
Optical rise/fall time	<3.0 ns.

References

ANSI Standard X3T1 1/ Levels FC-1 and FC-0.
DVB-PI-232 TM1449 Interfaces for CATV/SMATV Headends & similar Professional Equipment.
ETS 300 421. Digital broadcasting systems for Television, sound and data services; framing structure, channel coding for 11/12 GHz satellite services.
ETS 300 429. Digital broadcasting systems for Television, sound and data services; framing structure, channel coding and modulation for cable systems.
ETS 300 473. Digital broadcasting systems for Television, sound and data services; Satellite Master Antenna Television (SMATV) distribution systems.
ISO/IEC 13818-1 (Systems). MPEG-2 Standard.
ITU-T Rec. G.703.
TM 1664 Rev 2 - DVB Interfaces for PDH Networks.

Glossary of terms

8B/10B	Eight to Ten Bit Conversion.
ASI	Asynchronous Serial Interface.
ASI-C	ASI Coaxial cable.
ASI-O	ASI Fibre optic cable.
B3ZS	Bipolar with Three Zero Substitution.
BB	Baseband.
BER	Bit Error Rate.
CCIR	Comite Consultatif International des Radiocommunications.
CCITT	Comite Consultatif International Telephonique et Telegraphique.
CPLD	Custom Programmable Logic Device.
DJ	Deterministic Jitter.
DTVC	Digital Television by Cable.
DVB	Digital Video Broadcasting.
DVG	Digital Video Generator.
EBU	European Broadcasting Union.
EBU	European Broadcasting Union.
ETS	European Telecommunication Standard.
ETSI	European Telecommunications Standards Institute.
FEC	Forward Error Correction.
FIFO	First In First Out.
FPGA	Field Programmable Gate Array.
G.703	ITU CCITT recommendation G.703.
HDB3	High Density Bi-polar of order 3.
IF	Intermediate Frequency.
IRD	Integrated Receiver Decoder.
ITU	International Telecommunications Union.
LSB	Least Significant Bit.
LVDS	Low Voltage Differential Signalling.
Mb/s	Megabits per second.
MPEG	Moving Pictures Experts Group.
MPEG	Motion Picture Experts Group.
MSB	Most Significant Bit.
MSB	Most Significant Bit.
MUX	Multiplex.
NO	Normally open contact set.
NC	Normally closed contact set.
NRZ	Non Return to Zero.
PDH	Plesiochronic Digital Hierarchy.
PRBS	Pseudo Random Binary Sequence.
QAM	Quadrature Amplitude Modulation.
QEF	Quasi Error Free.
QPSK	Quarternary Phase Shift Keying.
R & S	Rohde & Schwarz.
RF	Radio Frequency.
RJ	Random Jitter.
RS	Reed Solomon.
SDI	Serial Digital Interface.
SMATV	Satellite Master Antenna Television.
SPI	Synchronous Parallel Interface MPEG2.
SSI	Synchronous Serial Interface.
TDM	Time Division Multiplex.
TS	Transport Stream.
TV	Television.

Drawing index

Unless otherwise specified all references on diagrams to the: DDC-3260 refer equally to the DDC-3261.
DDC-3270 refer equally to the DDC-3271.
DDC-3275 refer equally to the DDC-3276.

Drawing #	Sheet #	Description
804092		DDC-3260 circuit schematic.
804099		DDC-3270 circuit schematic.
804150		DDC-3275 circuit schematic.
804154		DDC-3320 circuit schematic.