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IRT Eurocard

Type MDC-3470

ASI to ASI/G.703
Network Interface Adapter

Designed and manufactured in Australia

IRT can be found on the Internet at:
http://www.irtelectronics.com

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Instruction Book

Table of Contents

This instruction book applies to units later than S/N 0208001.

Operational Safety:

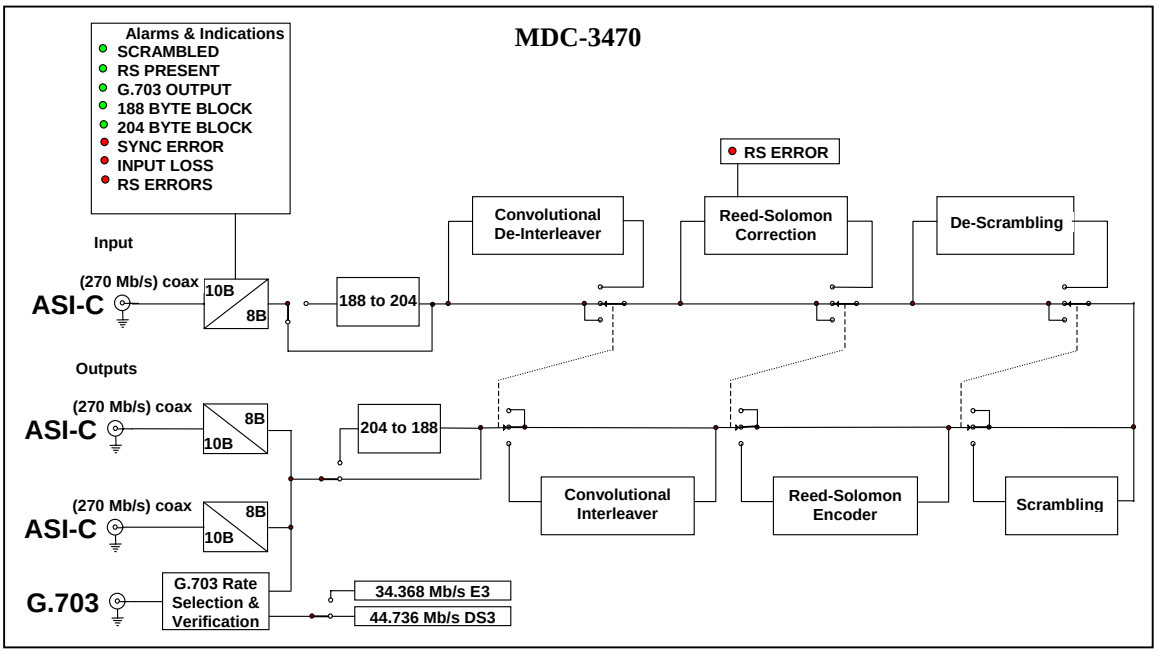
WARNING

Operation of electronic equipment involves the use of voltages and currents that may be dangerous to human life. Note that under certain conditions dangerous potentials may exist in some circuits when power controls are in the **OFF** position. Maintenance personnel should observe all safety regulations.

Do not make any adjustments inside equipment with power **ON** unless proper precautions are observed. All internal adjustments should only be made by suitably qualified personnel. All operational adjustments are available externally without the need for removing covers or use of extender cards.

IRT Eurocard
Type MDC-3470
ASI to ASI/G.703
Network Interface Adapter

General Description



The MDC-3470 is part of a family of data transcoders for converting between the commonly used MPEG2 Transport Stream formats in the broadcast industry for video distribution.

The MDC-3470 allows ASI to ASI conversion for any rate in the range of 2 Mb/s to 50 Mb/s and also allows Reed Solomon encoding/decoding, the insertion or removal of convolutional interleaving and MPEG2 transport stream scrambling/de-scrambling. It also allows rate adaption of 188 byte to 204 byte & 204 byte to 188 byte without requiring PCR re-stamping, i.e. no PCR error or stream modification. This makes it an ideal adjunct to test equipment or for matching signal from various sources using different encoding options.

The adapters find particular application interfacing for DVB-S applications compliant with ETSI 300-421, and CATV/SMATV Headends where equipment from different manufacturers uses different interfaces or where connection to test equipment is required from various sources.

The MDC-3470 accepts ASI input format only, but provides two simultaneous outputs in ASI format and in G.703 format. G.703 output is selectable between DS3 (44.736 kb/s) and E3 (34.368 kb/s), and is dependent on the output ASI stream being at the correct DS3 or E3 rate (see Table 1.1).

The MDC-3470 is fabricated in IRT's standard Eurocard format and may be housed in a variety of IRT's frames.

Applications:

- **Reed Solomon insertion & correction.**
- **Interleaving or de-interleaving.**
- **Scrambling or de-scrambling.**
- **Block length indication and error detection.**
- **Supplement to test equipment.**
- **188 to 204 & 204 to 188 byte conversion, where appropriate.**

Technical Specifications

IRT Eurocard module
Type/s MDC-3470

Input:

Type	1 x ASI, 75Ω ASI connector.
Rate	2 Mb/s to 50 Mb/s

Outputs:

Type	2 x ASI-C 75Ω, 800 mVp-p, BNC connector.
	1 x G.703, 75Ω BNC connector. HDB3 at 34 Mb/s or B3ZS at 45 Mb/s, selectable dependent on input ASI rate and on board link options equalling desired G.703 rate, see Table 1.1.
Power Requirements	28 Vac CT (14-0-14) or ± 16 Vdc.
Power consumption	~5 VA.

Other:

Temperature range		0 - 50° C ambient.
Mechanical		Suitable for mounting in IRT 19" rack chassis with input, output and power connections on the rear panel.
Finish:	Front panel	Grey background, silk-screened black lettering & red IRT logo.
	Rear assembly	Detachable silk-screened PCB with direct mount connectors to Eurocard and external signals.
Dimensions		6 HP x 3 U x 220 mm IRT Eurocard
Supplied accessories		Rear connector assembly including matching connector for alarm output.
Optional accessories		TME-6 module extender card

Due to our policy of continuing development, these specifications are subject to change without notice.

Technical Description

The MDC-3470 processes an ASI input and outputs processed ASI-C and G.703 at the input data rate.

This module is capable of performing scrambling, de-scrambling, RS encoding, RS decoding, interleaving and de-interleaving. It can encode as well as decode different MPEG TS formats. The module is normally set up as either a decoder or an encoder. Certain combinations of functions are inhibited (e.g. de-interleaving of a 188 byte transport stream with or without 188/204 conversion enabled).

The processing functions are selected using three switches (interleaving, RS coding and scrambling) on the front panel. Each switch has three positions (up, centre or down).

A switch set to the UP position applies processing to the decoding section.
A switch set to the DOWN position applies processing to the encoding section.
A switch set to the CENTRE position bypasses the decoding and encoding sections.

Applying a function to both the decoder and encoder section simultaneously is prevented mechanically by the switch. In most instances the MDC-3470 would be set to decoder mode with the de-interleaver and RS decoder functions enabled.

ASI Output
ASI operates at 270 Mbit/s and uses 8B/10B coding with K28.5 stuffing bytes. The ASI cable output uses a 75 Ohm BNC connector. A DVT-3211/DVR-3210 optical link can be used to transport the ASI-C signal via fibre optic cable. *See DVT-3211/DVR-3210 brochure or manual for further information.*

Input Loss Alarms
The Input Loss Alarm will be asserted in the absence of an ASI input.

Input TS Sync Error
After 2 consecutive TS syncs are missed a TS Sync Error is deemed to have occurred. The Sync error LED is turned off only after 5 consecutive TS syncs have been detected.

188 TS Packet length indicator
If the input TS packet length is 188 then the 188 LED lights (Note that 188 to 204 or 204 to 188 conversion will not affect this LED).

204 TS Packet length indicator
If the input TS packet length is 204 then the 204 LED lights (Note that 188 to 204 or 204 to 188 conversion will not affect this LED).

G703 Output
If the ASI rate at the input and the board links are as defined in Table 1.1 then the G703 output will be enabled. If the input data rate is outside the specified range then the G703 output will be muted.

OPERATION	Input Rate for valid G.703 Output (kb/s ± 20ppm)	
	E3 (LK1 IN)	DS3 (LK1 OUT)
No Rate Adaption (LK2 Out, LK3 Out)	34,368	44,736
188 → 204 (LK2 In)	31,672	41,227
204 → 188 (LK3 In)	37,292	48,543

Table 1.1: Input Rate for Valid G.703 Output

Alarm relay
Contacts from the Alarm relay are available on J2 of the rear assembly.
With LK7 out, the alarm condition is “Loss of ASI sync” – recommended configuration if using ASI outputs only.
With LK7 in, the Alarm condition is “No Valid G703 Output”.
The alarm condition is indicated by a short circuit between pins (1,2) and 4 of J2 (recommended), or open circuit between pins (1,2) and 3.

LED indicators
LED indicators 188 TS Byte length, 204 TS Byte length, R-S error, Scram present, R-S present are blanked during Input loss or sync loss.

Configuration

Links & options:

Warning:
Some of the following links are for factory use only and should not be changed.
Links may be changed without disconnecting power. However, when any link is changed, normal decoding of the MPEG TS will be disturbed. The time taken before normal decoding resumes is dependent on the decoder in use and may be up to five seconds.

LK 1	OUT	DS3 (44.736 Mb/s) G.703 operation.
	IN	E3 (34.368 Mb/s) G.703 operation.
LK 2	IN	188 to 204 byte translation.
LK 3	IN	204 to 188 byte translation.
LK 4	Reserved for future use.	
LK 5	IN	TEI* bit (Transport Error Indicator) assertion active.
LK 6	Reserved for future use.	
LK 7	IN	The Alarm condition is “No Valid G703 Output”.
	OUT	The alarm condition is “Loss of ASI sync”.

Note that for a 188 byte input signal, LK2 must be installed for full encoding functionality (Reed Solomon, Interleaving).

CAUTION: Do not have both links LK2 and LK3 in at the same time.

* TEI – b7 of byte after sync byte.
If set, indicates current packet contains uncorrectable RS errors.
This bit is set by the MDC-3470 if LK5 is IN, the RS decoder is operating, Scrambling is not present and uncorrectable RS errors are detected in the current packet.

Installation

Pre-installation:

Handling:

This equipment may contain or be connected to static sensitive devices and proper static free handling precautions should be observed.

Where individual circuit cards are stored, they should be placed in antistatic bags. Proper antistatic procedures should be followed when inserting or removing cards from these bags.

Power:

AC mains supply: Ensure that operating voltage of unit and local supply voltage match and that correct rating fuse is installed for local supply.

DC supply: Ensure that the correct polarity is observed and that DC supply voltage is maintained within the operating range specified.

Earthing:

The earth path is dependent on the type of frame selected. In every case particular care should be taken to ensure that the frame is connected to earth for safety reasons. See frame manual for details.

Signal earth: For safety reasons a connection is made between signal earth and chassis earth. No attempt should be made to break this connection.

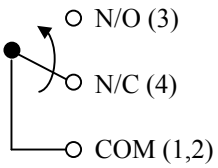
Installation in frame or chassis:

See details in separate manual for selected frame type.

Input/Output & alarm connections:

ASI input and ASI & G.703 outputs are by 75Ω BNC connectors on the rear assembly.

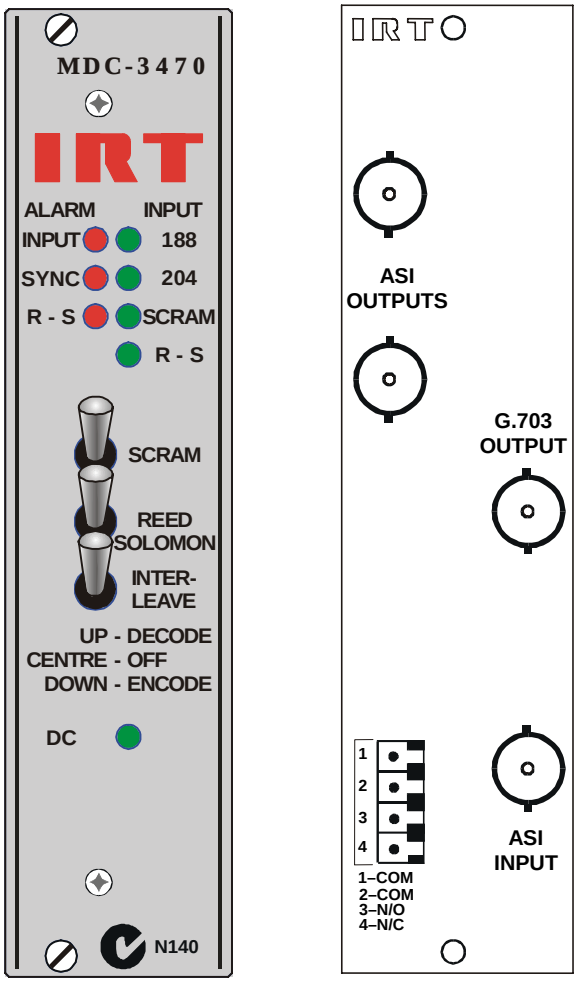
Alarm output is by a 4-pin Phoenix style screw connector on the rear assembly. Alarm is by a relay contact. N/O, N/C and two COM connections are provided.



With LK7 out, the alarm condition is “Loss of ASI sync”.
With LK7 in, the Alarm condition is “No Valid G703 Output”.
The alarm condition is indicated by a short circuit between pins 1 and 4 of J2.

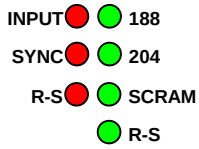
Front & rear panel connector diagrams

The following front panel and rear assembly drawings are not to scale and are intended to show connection order and approximate layout only.



Operation

Front Panel Indicators:



Input loss alarm:
This LED lights when no data is detected at the input.

Sync loss alarm:
This LED lights when two or more contiguous MPEG-2 TS sync bytes are absent. The LED extinguishes when five or more contiguous correct SYNC bytes are detected.

188 byte indicator:
This LED lights when a valid MPEG-2 TS with 188 byte packet length is input.

204 byte indicator:
This LED lights when a valid MPEG-2 TS with 204 byte packet length is input.

Scrambling presence indicator:
This LED lights when a valid MPEG-2 TS stream containing a byte sequence that corresponds to scrambling. A scrambling byte sequence uses an inverted 47H sync byte (B8H) every eighth sync to signify the start of the scrambling sequence.

R-S (Reed Solomon) presence indicator (Green):
This LED lights when Reed Solomon error correction bytes are present in place of the 16 dummy bytes of a 204 Byte MPEG-2 TS. The MDC-3470 considers any data content other than all 0's during the 16 dummy bytes to be RS correction bytes.

R-S (Reed Solomon) Error indicator (Red):
This LED lights for at least 300 ms when un-correctable R-S packets are detected. These correspond to packets with more than 8 bytes in error.

Processing controls:

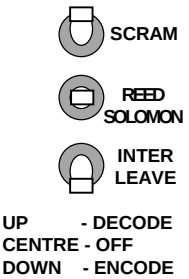
This module is capable of performing scrambling, de-scrambling, RS encoding, RS decoding, interleaving and de-interleaving.

In this context, the word scrambling refers to the process of randomisation for the purpose of energy dispersal of the signal. It does not refer to the encryption applied to Pay TV signals to control access to particular channels or programs.

For a description of the processes involved see *Application examples - Cable Systems* and *Technical specifications - Characteristics of signal types - MPEG-2 transport layer coding*.

The module is normally set up as either a decoder or an encoder. Combinations of both functions simultaneously should be avoided.

The processing functions are selected using three switches (interleaving, RS coding and scrambling) on the front panel. Each switch has three positions (up, centre or down).



A switch set to the UP position applies processing to the decoding section;
a switch set to the DOWN position applies processing to the encoding section; and
a switch set to the CENTRE position does not perform that function to either the decoding or encoding section.

In most instances, the MDC-3470 would be set to all encode or all decode.

Maintenance & storage

Maintenance:

No regular maintenance is required.

Care however should be taken to ensure that all connectors are kept clean and free from contamination of any kind. This is especially important in fibre optic equipment where cleanliness of optical connections is critical to performance.

Storage:

If the equipment is not to be used for an extended period, it is recommended the whole unit be placed in a sealed plastic bag to prevent dust contamination. In areas of high humidity a suitably sized bag of silica gel should be included to deter corrosion.

Where individual circuit cards are stored, they should be placed in antistatic bags. Proper antistatic procedures should be followed when inserting or removing cards from these bags.

Warranty & service

Equipment is covered by a limited warranty period of three years from date of first delivery unless contrary conditions apply under a particular contract of supply. For situations when "**No Fault Found**" for repairs, a minimum charge of $A100.00 will apply, whether the equipment is within the warranty period or not.

Equipment warranty is limited to faults attributable to defects in original design or manufacture. Warranty on components shall be extended by IRT only to the extent obtainable from the component supplier.

Equipment return:

Before arranging service ensure that the fault is in the unit to be serviced and not in associated equipment. If possible, confirm this by substitution.

Before returning equipment contact should be made with IRT or your local agent to determine whether the equipment can be serviced in the field or should be returned for repair.

The equipment should be properly packed for return observing antistatic procedures.

The following information should accompany the unit to be returned:

1. A fault report should be included indicating the nature of the fault
2. The operating conditions under which the fault initially occurred.
3. Any additional information which may be of assistance in fault location and remedy.
4. A contact name and telephone and fax numbers.
5. Details of payment method for items not covered by warranty.
6. Full return address.
7. For situations when "**No Fault Found**" for repairs, a minimum charge of $A100.00 will apply, whether the equipment is within the warranty period or not.

Please note that all freight charges are the responsibility of the customer.

The equipment should be returned **to the agent who originally supplied the equipment or, where this is not possible**, to IRT direct as follows.

Equipment Service
IRT Electronics Pty Ltd
26 Hotham Parade
ARTARMON
N.S.W. 2064
AUSTRALIA

Phone: 61 2 9439 3744 Fax: 61 2 9439 7439
Email: service@irtelectronics.com

Characteristics of signal types

Coding characteristics

G.703:

The **HDB3** (High Density Bi-polar of order 3) code as defined in G.703 for 34,368 kbits/s is as follows:

Binary 1 bits are represented by alternate positive and negative pulses and binary 0 bits by spaces. Exceptions are made when strings of successive 0 bits occur in the binary signal.

Each block of 4 successive zeros is replaced by 000V or B00V where B is an inserted pulse of the correct polarity and V is an inserted pulse violating the polarity rule. The choice of 000V or B00V is made so that the number of B pulses between consecutive V pulses is odd so that successive V pulses are of alternate polarity and so no DC component is introduced.

The **B3ZS** (Bipolar with Three Zero Substitution) (Also designated **HDB2** - High Density Bi-polar of order 2) code as defined in G.703 for 44,736 kbits/s is as follows:

Binary 1 bits are represented by alternate positive and negative pulses and binary 0 bits by spaces. Exceptions are made when strings of successive 0 bits occur in the binary signal.

Each block of 3 successive zeros is replaced by 00V or B0V. The choice of 00V or B0V is made so that the number of B pulses between consecutive V pulses is odd, so that successive V pulses are of alternate polarity and so no DC component is introduced.

Asynchronous Serial Interface (ASI)

The Asynchronous Serial Interface (ASI) provides a system for serial encoded transmission of different data rates with a constant transmission rate of 270 Mbit/s.
The ASI standard supports coaxial cable and multi-mode fibre-optic cable (using LED emitters).

ASI Protocol Architecture Description

The ASI protocol is divided into three architectural layers: Layer-0, Layer-1 and Layer-2.
MPEG Transport Packets form the top layer (Layer 2), and the bottom layers are based upon the Fibre Channel Standard (Layers 1 and 0). Layer 2 is defined using the MPEG-2 Standard ISO/IEC 13818-1 (Systems). Layers 1 and 0 are based upon a subset of ANSI Standard X3T11/ Levels FC-1 and FC-0.

Layer-O: Physical Requirements

The physical Layer defines the transmission media, the drivers and receivers, and the transmission speeds. The physical interface provides for both LED-driven multimode fibre and copper coaxial cable.

Line Rates and Bit Timing

The encoded line rate with the 8B/10B block code is 270 Mbit/s which results in a media transmission rate of 270 MBaud. At the transmitter, the serialisation is done using a fixed oscillator to establish this 270 MBaud rate from which a phase-locked Byte clock is derived and used to shift in parallel Bytes.

Receivers recover the serial transmission clock. A phase-locked Byte clock is derived from this recovered serial bit clock and is used to shift parallel Bytes out to Layer- 1 processing elements. It is required that the encoded line rate shall be 270 MBaud ±100 ppm.

Layer-1 Data Encoding

The ASI Transmission Layer 1 deals with encoding/decoding aspects, which are independent of the transmission medium characteristics. The encoding method utilised is specified in the fibre channel document X3T11

At Layer-1, Bytes are 8B/10B coded, which produces one 10-bit word for each 8-bit Byte presented.
The 8B/10B transmission coding provides for both a self checking capability and Byte synchronisation of the link. The 10B transmission code is defined in terms of "disparity": the difference in the number of "1" bits and "0" bits in the transmitted serial data stream. The disparity characteristics of the code maintain DC balance.
Special characters are defined as extra code points beyond the need to encode a Byte of data. One in particular is used to establish Byte synchronisation in the ASI transmission link.

The 10-bit words are then passed through a parallel-to-serial converter, which operates at a fixed output bit-rate of 270 Mbit/s. If the converter requests a new input word and the data source does not have one ready, a synchronisation word is inserted. These sync words are ignored by receive equipment.
The resulting serial bit stream is passed to the output driver circuit for coaxial or fibre-optic cable.

Receive data arriving on a coaxial cable or fibre is first coupled to a circuit, which recovers clock and data.
Recovered serial data bits are passed to a 10B/8B decoder that converts the 10-bit transmission words back into the 8-bit Bytes originally transmitted. In order to recover Byte alignment, the 10B/8B decoder initially searches for synchronisation words. Once found, the start of the synchronisation word marks the boundary of subsequent received data words and establishes proper Byte-alignment of decoder output Bytes.

NOTE - The ASI coding is sensitive to logical inversion of the transmitted bits. Therefore, to ensure correct operation, care must be taken that equipment interface circuitry of the non-inverting type is used.

The **Bit-Error-Rate (BER) Performance** shall be less than one part in 10^{13}.

Layer-2 Transport Protocol

The ASI Transmission Layer-2 standard uses the MPEG-2 Transport Stream Packet as defined in ISO/IEC 13818-1 (Systems) as its basic message unit. Optionally the RS coded Byte structure as specified in ETS 300 429 is also supported.

Data to be transmitted are presented in Byte-synchronised form as MPEG-2 Transport packets. Transport Packets may be presented to Layer-2 either as a burst of contiguous Bytes, or as individual Bytes spread out in time.

The ASI Interface Layer-2 definition employs the MPEG-2 Transport Stream packet syntax with the additional requirement that every Transport Packet shall be preceded with at least two synchronisation characters. This allows re-sync within one transport packet in the event that a line disturbance causes loss of sync.

MPEG-2 transport layer coding

The MPEG-2 Transport Layer is defined in ISO/IEC DIS 13818-1 [1]. The Transport Layer for MPEG-2 data is comprised of packets having 188 Bytes, with one Byte for synchronisation purposes, three Bytes of header containing service identification, scrambling and control information, followed by 184 Bytes of MPEG-2 or auxiliary data.
The framing organisation is based on the MPEG-2 transport packet structure.

Channel coding

Randomisation for spectrum shaping (Scrambling)
The System input stream is organised in fixed length packets (see figure 2), following the MPEG-2 transport multiplexer. The total packet length of the MPEG-2 transport MUX packet is 188 Bytes. This includes 1 sync-word Byte (i.e. 47_{HEX}). The processing order at the transmitting side shall always start from the MSB (i.e. 0) of the sync word-Byte (i.e. 01000111).

In order to comply with the System for satellite, (see ETS 300 421) and to ensure adequate binary transitions for clock recovery, the data at the output of the MPEG-2 transport multiplex is randomised.

The polynomial for the Pseudo Random Binary Sequence (PRBS) generator is:

$1 + X^{14} + X^{15}$

Loading of the sequence 100101010000000" into the PRBS registers, is initiated at the start of every eight transport packets. To provide an initialisation signal for the de-scrambler, the MPEG-2 sync Byte of the first transport packet in a group of eight packets is bitwise inverted from 47_{HEX} to $B8_{HEX}$.

The first bit at the output of the PRBS generator is applied to the first bit of the first Byte following the inverted MPEG-2 sync Byte (i.e.$B8_{HEX}$). To aid other synchronisation functions, during the MPEG-2 sync Bytes of the subsequent 7 transport packets, the PRBS generation continues, but its output is disabled, leaving these Bytes unrandomised. The period of the PRBS sequence shall therefore be 1,503 Bytes.

The randomisation process is active also when the modulator input bit-stream is non-existent, or when it is non-compliant with the MPEG-2 transport stream format (i.e. 1 sync Byte + 187 packet Bytes). This is to avoid the emission of an unmodulated carrier from the modulator.

Reed-Solomon coding
Following the energy dispersal randomisation process, systematic shortened Reed-Solomon encoding is performed on each randomised MPEG-2 transport packet, with T = 8. This means that 8 erroneous Bytes per transport packet can be corrected. This process adds 16 parity Bytes to the MPEG-2 transport packet to give a codeword (204, 188).

NOTE: RS coding is applied also to the packet sync Byte, either non-inverted (i.e. 47_{HEX}) or inverted (i.e. $B8_{HEX}$).

Code Generator Polynomial: $g(x) = (x+\lambda^0)(x+\lambda^1)(x+\lambda^2) \ldots (x+\lambda^{15})$, where $\lambda = 02_{HEX}$

Field Generator Polynomial: $p(x) = x^8 + x^4 + x^3 + x^2 + 1$

The shortened Reed-Solomon code is implemented by appending 51 Bytes, all set to zero, before the information Bytes at the input of a (255, 239) encoder; after the coding procedure these Bytes are discarded.

Convolutional interleaving
Convolutional interleaving with depth I = 12 is applied to the error protected packets (see figure 2c). This results in an interleaved frame.

The convolutional interleaving process is based on the Forney approach which is compatible with the Ramsey type III approach, with I = 12. The Interleaved Frame is composed of overlapping error-protected packets and is delimited by MPEG-2 sync Bytes (preserving the periodicity of 204 Bytes).

The interleaver may be composed of I = 12 branches, cyclically connected to the input Byte-stream by the input switch. Each branch is a First In First Out (FIFO) shift register, with depth (Mj) cells (where M = 17 = N/I, N = 204 = error protected frame length, I = 12 = interleaving depth, j = branch index). The cells of the FIFO shall contain 1 Byte, and the input and output switches is synchronised.

For synchronisation purposes, the sync Bytes and the inverted sync Bytes are always routed into the branch 0" of the interleaver (corresponding to a null delay).

The de-interleaver is similar, in principle, to the interleaver, but the branch indexes are reversed (i.e. j = 0 corresponds to the largest delay). The de-interleaver synchronisation can be carried out by routing the first recognised sync Byte into the "0" branch.

The purpose of the interleaver is to improve the R-S decoder performance when the system is subject to burst errors, i.e. a long string of successive errors that occur only occasionally. The interleaver shuffles data in packets (after R-S decoding) effectively redistributing the 204 bytes of data over a period of time equivalent to many packet durations. The deinterleaver does the reverse. Hence a long string of errors in an interleaved stream will be redistributed to a small number of errors per packet over a long period of time. Since the R-S decoder can handle up to 8 byte errors per 204 byte packet, the R-S output will now be error free. If interleaving was not used, a burst of 9 errors in a packet would cause that packet to be lost (marked un-correctable & hence be ignored by down stream equipment).

General Information on DVB-ASI

For transport, the 270 Mb/s stream may be fed through DA's and switchers without regard for the underlying data rate, thus simplifying system design.
Note that the ASI signal is polarity sensitive. Although most 270 Mb/s SDI DA's and switchers will pass ASI signals, the line drivers used usually have both inverted and non-inverted outputs. For ASI, only those outputs that are non-inverted may be used.

Electrical characteristics ASI:

Transmitter output characteristics:

Output voltage	800 mVp-p ±10%.
Deterministic jitter	<10% p-p.
Random jitter	<8% p-p.
Rise/fall time (20-80%)	<1.2 ns.

Receiver input characteristics:

Minimum sensitivity (D21.5 idle pattern)	200 mV
Maximum input voltage	880 mVp-p
Minimum discrete connector return loss	15 dB (5 MHz - 270 MHz)

Coaxial link:

Impedance	75 Ohm
Equipment connector	BNC female

(Electrical measurements made with 75 Ohm resistive termination.)

References

ANSI Standard X3T1 1/ Levels FC-1 and FC-0.
DVB-PI-232 TM1449 Interfaces for CATV/SMATV Headends & similar Professional Equipment.
ETS 300 421. Digital broadcasting systems for Television, sound and data services; framing structure, channel coding for 11/12 GHz satellite services.
ETS 300 429. Digital broadcasting systems for Television, sound and data services; framing structure, channel coding and modulation for cable systems.
ETS 300 473. Digital broadcasting systems for Television, sound and data services; Satellite Master Antenna Television (SMATV) distribution systems.
ISO/IEC 13818-1 (Systems). MPEG-2 Standard.
ITU-T Rec. G.703.
TM 1664 Rev 2 - DVB Interfaces for PDH Networks.

Glossary of terms

8B/10B	Eight to Ten Bit Conversion.
ASI	Asynchronous Serial Interface.
ASI-C	ASI Coaxial cable.
ASI-O	ASI Fibre optic cable.
B3ZS	Bipolar with Three Zero Substitution.
BB	Baseband.
BER	Bit Error Rate.
CCIR	Comite Consultatif International des Radiocommunications.
CCITT	Comite Consultatif International Telephonique et Telegraphique.
CPLD	Custom Programmable Logic Device.
DJ	Deterministic Jitter.
DTVC	Digital Television by Cable.
DVB	Digital Video Broadcasting.
DVG	Digital Video Generator.
EBU	European Broadcasting Union.
EBU	European Broadcasting Union.
ETS	European Telecommunication Standard.
ETSI	European Telecommunications Standards Institute.
FEC	Forward Error Correction.
FIFO	First In First Out.
FPGA	Field Programmable Gate Array.
G.703	ITU CCITT recommendation G.703.
HDB3	High Density Bi-polar of order 3.
IF	Intermediate Frequency.
IRD	Integrated Receiver Decoder.
ITU	International Telecommunications Union.
LSB	Least Significant Bit.
LVDS	Low Voltage Differential Signalling.
Mb/s	Megabits per second.
MPEG	Moving Pictures Experts Group.
MPEG	Motion Picture Experts Group.
MSB	Most Significant Bit.
MSB	Most Significant Bit.
MUX	Multiplex.
NO	Normally open contact set.
NC	Normally closed contact set.
NRZ	Non Return to Zero.
PDH	Plesiochronic Digital Hierarchy.
PRBS	Pseudo Random Binary Sequence.
QAM	Quadrature Amplitude Modulation.
QEF	Quasi Error Free.
QPSK	Quarternary Phase Shift Keying.
R & S	Rohde & Schwarz.
RF	Radio Frequency.
RJ	Random Jitter.
RS	Reed Solomon.
SDI	Serial Digital Interface.
SMATV	Satellite Master Antenna Television.
SPI	Synchronous Parallel Interface MPEG2.
SSI	Synchronous Serial Interface.
TDM	Time Division Multiplex.
TS	Transport Stream.
TV	Television.

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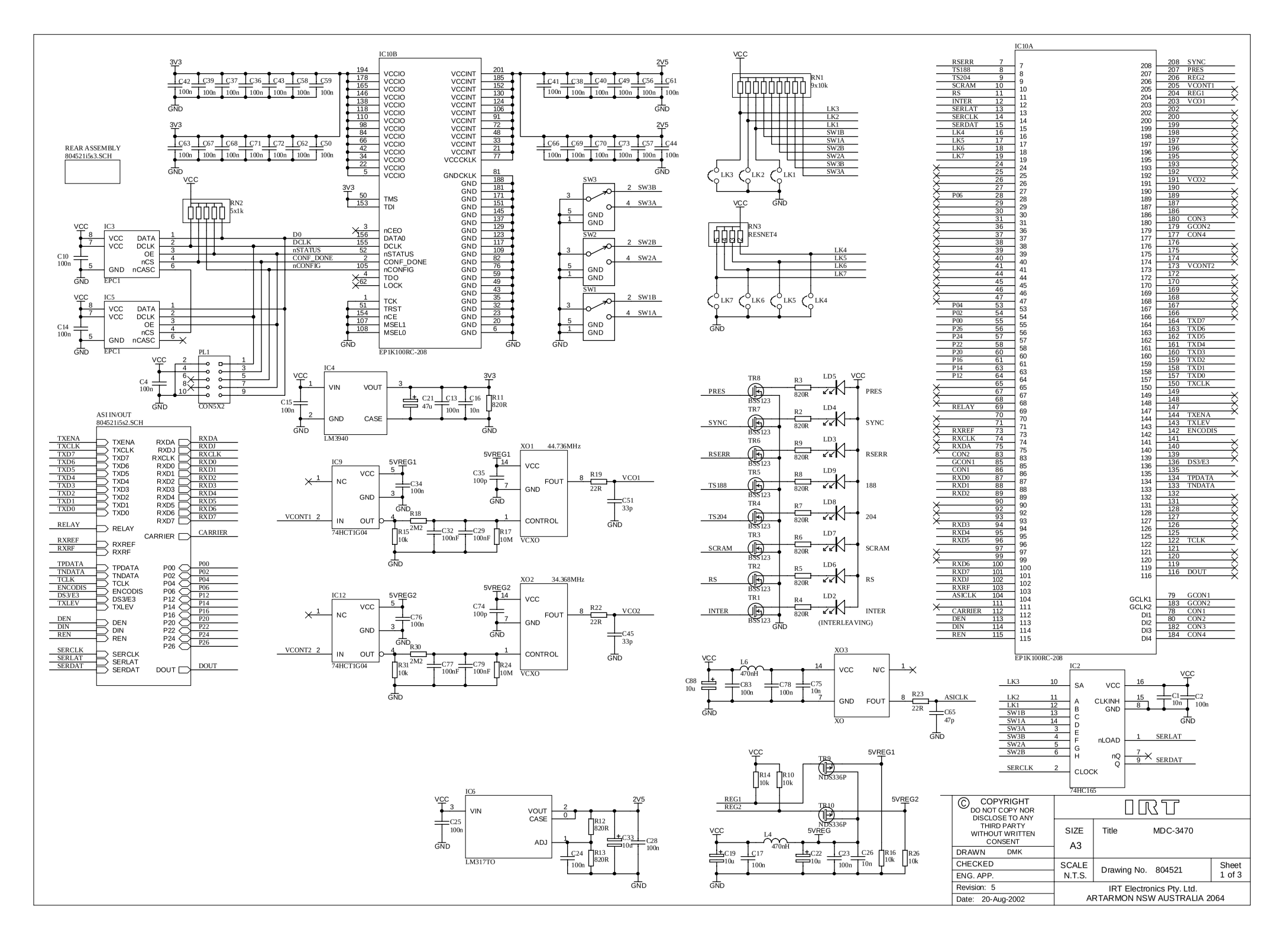
804521	3	MDC-3470 circuit diagram – sheet 3



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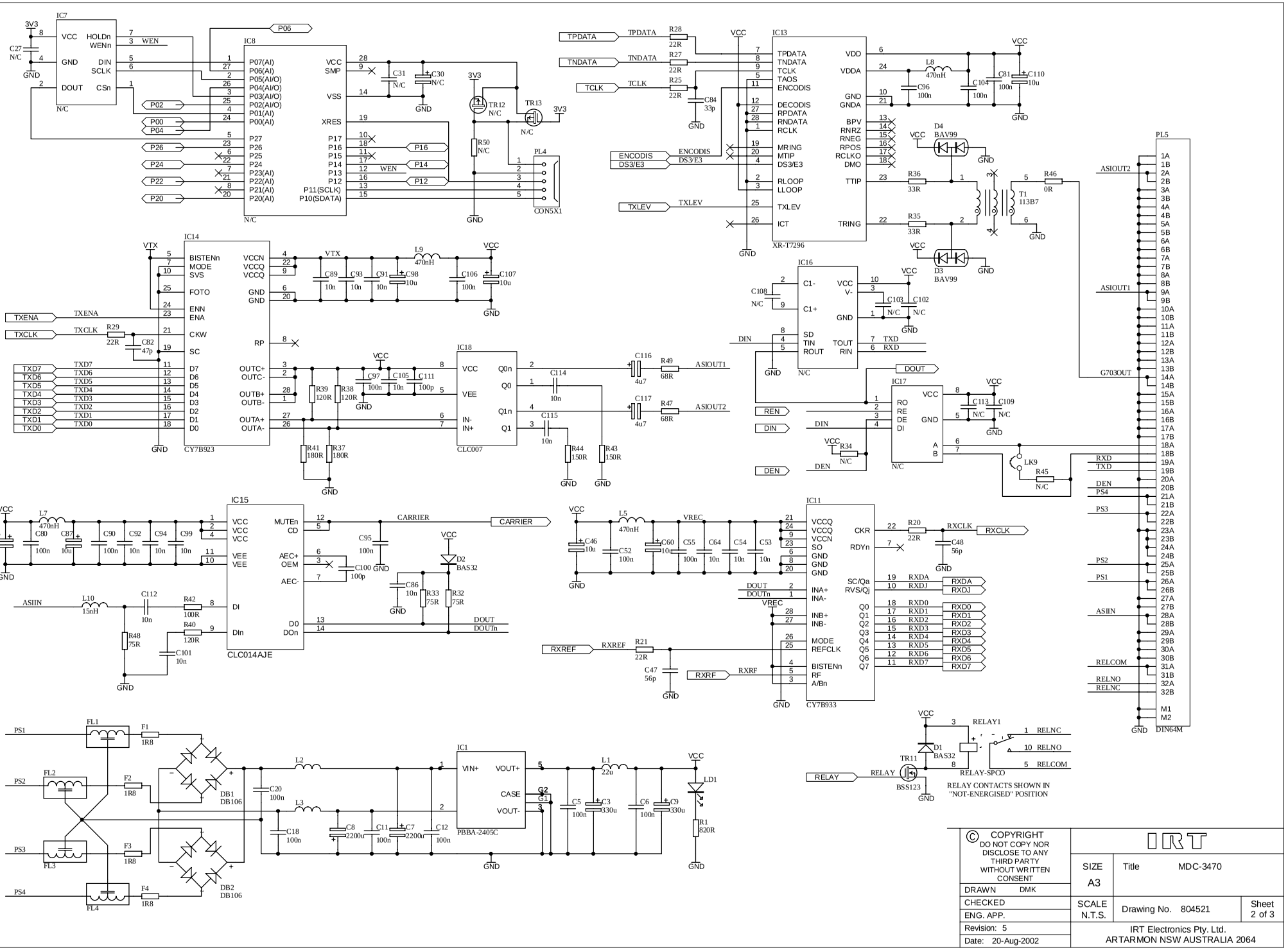

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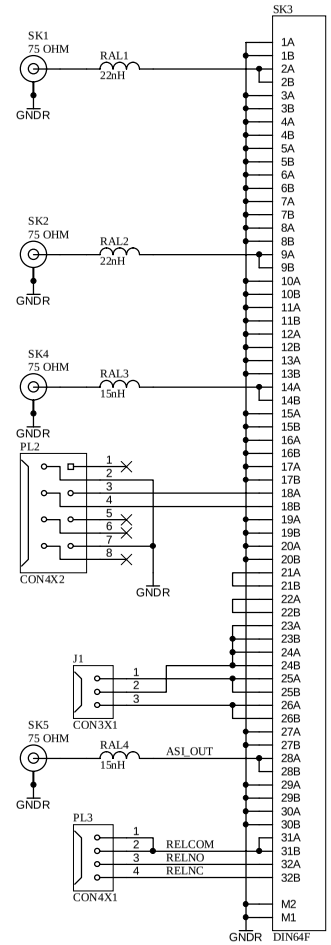

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