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IRT Eurocards

Types MDT-3510 & MDR-3510

SPI to 70 MHz IF QPSK Encoder & Decoder System

Designed and manufactured in Australia

IRT can be found on the Internet at:
http://www.irtelectronics.com

IRT Eurocards

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Instruction Book

Table of Contents

This instruction book applies to units later than S/N 0111001.

Operational Safety:

WARNING

Operation of electronic equipment involves the use of voltages and currents that may be dangerous to human life. Note that under certain conditions dangerous potentials may exist in some circuits when power controls are in the **OFF** position. Maintenance personnel should observe all safety regulations.

Do not make any adjustments inside equipment with power **ON** unless proper precautions are observed. All internal adjustments should only be made by suitably qualified personnel. All operational adjustments are available externally without the need for removing covers or use of extender cards.

IRT Eurocards
Types MDT-3510 & MDR-3510
SPI to 70 MHz IF QPSK
Encoder & Decoder System

General Description

The MDT-3510 and MDR-3510 form a 70 MHz IF QPSK encoder/decoder system allowing existing analogue (FM) microwave systems to carry MPEG transport streams. It is specifically designed to work with the non-linear power amplifiers commonly used for FM systems and will tolerate a large amount of microwave LO phase noise.

The MDT-3510 transmitter accepts a 12 Mb/s to 49 Mb/s SPI input signal and outputs a QPSK encoded signal centred at 70 MHz. The bandwidth of the output is directly related to the input data rate & the Viterbi FEC (forward error correction) selected by on board switches. This allows the user maximum flexibility when restricted to a nominated microwave link bandwidth.

The MDT-3510 is designed to interface with the DDC-3335, allowing 188 byte or 204 byte ASI input streams to be used.

Output RF level is controllable from the front panel with an adjustment range greater than 20 dB. A monitoring port is provided on the front panel for connection to test equipment. The output is DVB-S compliant.

The MDR-3510 receiver will decode an appropriate QPSK signal to give an SPI output formatted as 204 byte data.

The MDR-3510 has RF automatic gain control with a range greater than 20 dB. The unit automatically performs Viterbi decoding, RS error correction, de-interleaving and de-scrambling.

For a link situation, an onboard jumper (SW1-7 OFF) configures the output so that it can be directly connected to an MDT-3510 for retransmission. This allows multiple hops to be performed without error accumulation and with a minimum of equipment.

The MDT-3510, MDR-3510 and corresponding affiliate cards are suitable for mounting in all IRT's standard 1RU and 3RU frames

Standard features:

- **Allows existing analogue microwave links to carry digital encoded signals.**
- **Accepts symbol rates from 12 to 28 Msymbols/s (12 to 49 Mb/s - dependent on selected Viterbi).**
- **Encodes and decodes MPEG TS signals into 70 MHz IF QPSK modulated signals.**
- **RF level controllable from front panel.**
- **Selectable Viterbi FEC – 1/2, 2/3, 3/4, 5/6, 7/8.**
- **Bandwidth (BW) determined only by Input rate and Output Viterbi FEC selection.**

Technical Specifications

IRT Eurocard module
MDT-3510 / MDR-3510

MDT-3510

Input: 1 x SPI, 204 byte, RS encoded, interleaved and scrambled (12 - 49 Mb/s.)

Electrical characteristics	LVDS drivers.
Connector	25 pin 'D' female type.
Viterbi Switch	Select 1/2, 2/3, 3/4, 5/6, 7/8.

Output: 1 x 70 MHz IF RF QPSK encoded.

Connector	BNC, 75 Ω.
Maximum output power	-5dBm

Alarms:

1 x general alarm - Sync error / input loss/ power loss.
1 set relay contacts - N/O, N/C, Com
4 pin phoenix style connector.

MDR-3510

Input: 1 x 70 MHz IF RF QPSK encoded.

Connector	BNC, 75 Ω.

Output: 1 x SPI, 204 bye, RS decoded, de-interleaved and de-scrambled.

Electrical characteristics	LVDS drivers.
Connector	25 pin 'D' female type.

Alarms:

1 x general alarm - Sync error / input loss/ power loss.
1 set relay contacts - N/O, N/C, Com
4 pin phoenix style connector.

Power Requirements	28 Vac CT (14-0-14) or ± 16 Vdc.
Power consumption	<7 VA.

Other:

Temperature range		0 - 50° C ambient
Mechanical		Suitable for mounting in IRT 19” rack chassis with input, output and power connections on the rear panel.
Finish:	Front panel	Grey enamel, silk-screened black lettering & red IRT logo
	Rear assembly	Detachable silk-screened PCB with direct mount connectors to Eurocard and external signals
Dimensions		6 HP x 3 U x 220 mm IRT Eurocard
Supplied accessories		Rear connector assembly including matching connector for alarm output.
Related products		DDC-3335 ASI (188 byte) to SPI (204 byte) converter with RS insertion, interleaving and scrambling, DDC-3340 SPI to ASI converter, MFC-3540 SPI (204 byte) to ASI (188 byte) converter.
Optional accessories		TME-6 module extender card

Due to our policy of continuing development, these specifications are subject to change without notice.

Relationship of Data Rate to Channel Bandwidth

This discussion includes the overhead contributed by the Viterbi FEC and additional RS encoded bytes.

For a Channel Bandwidth (at –3dB) = BW, the maximum effective bandwidth is usually considered to be between BW/ 1.2 and BW/ 1.3. This takes into account the excess bandwidth required by the raised cosine filtering as well as allowing a suitable margin for signal degradation due to transponder bandwidth limitations. Hence the maximum effective symbol rate that can be transmitted is **Rs = BW/1.2.= 0.83 BW**

The incoming data rate **Ri** (MPEG Transport Stream with 188 byte format) has Reed-Solomon coding bytes appended to it. This increases the packet length to 204 bytes. Hence the encoded data rate **Re = 204/188 Ri**.

The interleaving and scrambling operations do not contribute any additional data to the stream, they just disperse and randomise the bits in the stream to improve FEC performance at the receiver.

The Viterbi FEC contributes redundant information to protect the data stream. The amount of redundant data added is dependent upon the selected Viterbi Rate (VR). The output data stream rate is inversely proportional to the Viterbi rate – e.g. VR = 2/3 will result in an output data rate Ru = 3/2 Re.

Since the QPSK modulator uses 2 bits to represent each symbol, the effective data output rate Ru = 2 Rs.

These relationships are summarized below :

Rs = 0.83 BW
Ru = 2 x Rs
Re = VR x Ru
Ri = (188/204) x Re

Hence the relationship between input data rate and effective IF output data rate can be shown to be :

Ri = 188/204 x VR x 2 x 0.83 x BW

The effective data rates for a 28 MHz (at –3dB) bandwidth channel, relative to the selected Viterbi rate, is tabulated below:

Viterbi Rate	Re – Effective Rate in 204 byte packet mode (Mbps)	Equivalent 188 format Data Rate (Mbps)
1/2	23.33	21.50
2/3	31.11	28.67
3/4	35.00	32.25
5/6	38.89	35.84
7/8	40.83	37.63

Effective Input Data Rate for a 28MHz (-3dB) Channel Bandwidth

Note that Ri, the effective input data may be considered to be a MPEG Transport Stream with 188 byte packet length. Re is the rate of the equivalent MPEG Transport Stream after conversion to a 204 byte packet length.

Configuration

MDT-3510 User Interface :

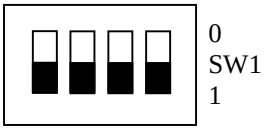
The MDT-3510 QPSK modulator board allows the user to select the required Viterbi FEC (forward error correction), set the output RF level, and have some control over the filtering of the output signal.

Viterbi Selection :

SW1 consists of 4 independent SPST switches. The silkscreen legend on the board identifies switches B2, B1 and B0 and indicates the correct settings for the desired Viterbi FEC selection. Switch A has no effect on the modules functional performance.

B2	B1	B0	Viterbi FEC
0	0	0	1/2
0	0	1	2/3
0	1	0	3/4
0	1	1	5/6
1	X	X	7/8

Here X is a “Don’t Care” condition. The position of the switch for logic 1 is also shown on the silkscreen legend.



Note:

- Rate 1/2 Viterbi provides the greatest error protection (adds one bit of FEC for every data bit). After 1/2 rate encoding the output data rate = 2 x input data rate.
- Rate 7/8 Viterbi provides the least error protection (adds one bit of FEC for every 7 data bits). After 7/8 rate encoding, the output data rate = 8/7 x input data rate.

RF Output Level Adjust :

The Potentiometer RV1 allows the user to adjust the RF output level by more than 20dB, to a maximum level of -5dBm. The Output Level Monitor 75ohm BNC on the front panel allows a spectrum analyser or RF Power meter to be connected, allowing the level to be adjusted with the module installed in situ. Note that the Output Level Monitor connector is nominally -10dB with respect to the rear ancillary output level.

Fine Bandwidth Adjust :

The Potentiometer RV2 allows the low pass filter cut-off frequency to be modified. This can be used to reduce QPSK out-of band spectral components. With a spectrum analyser connected at either the output BNC connector on the rear assembly or the Output level monitor on the front panel, RV2 can be adjusted to reduce the level of the out of band spectral components. Note that coarse filter selection is performed automatically by the unit based on the input SPI clock rate.

Important:
For some input rates, it may be possible to adjust RV2 such that the filter shapes the main lobe itself. This is not desirable and will result in increased link error rates. Care should be taken in adjustment of this potentiometer.

MDR-3510 User Interface:

The MDR-3510 requires the user to select the operating Symbol Rate, and allows the user to select various RS-485 error logging interface characteristics. The board may also be set in a "Link" mode (SW1-7 OFF) to allow it to be used prior to another MDT-3510 in a retransmission mode of operation.

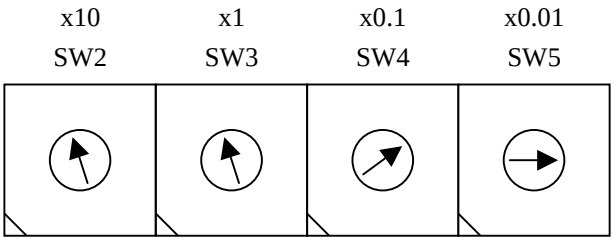
Symbol Rate Selection Switches SW2, SW3, SW4, SW5:

$$\text{Symbol Rate} = \tfrac{1}{2} \times (\text{Bit Rate}) \times (1/\text{Viterbi Rate})$$

Bit Rate corresponds to the output bit rate, which is a 204 byte packet length stream.

Switches SW2, SW3, SW4 and SW5 (if fitted) need to be set by the user to the desired operating symbol rate. The switches are Binary Coded Decimal (BCD) with the following scale factors (as indicated by the silkscreen legend on the PCB):

SW2 – 10 Msymbols/s
SW3 – 1 Msymbols/s
SW4 – 0.1 Msymbols/s
SW5 – 0.01 Msymbols/s (if fitted)



Hence to set 22.45 Msymbols/s operation - SW2 = 2, SW3 = 2, SW4 = 4 and SW5 = 5 (if fitted). Greater accuracy is not required for the system to lock.

Configuration DIP switch SW1

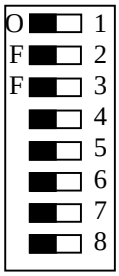
This consists of 8 SPST switches that allow various operating parameters to be set. DIP switches are read only at power on (also see LK1 jumper below). These are discussed below:

SW1-1 RS-485 Address ADD3 – MSB. When ON ADD3 =1. Else ADD3 = 0.
SW1-2 RS-485 Address ADD2. When ON ADD2 =1. Else ADD2 = 0.
SW1-3 RS-485 Address ADD1. When ON ADD1 =1. Else ADD1 = 0.
SW1-4 RS-485 Address ADD0 - LSB When ON ADD0 =1. Else ADD0 = 0.

SW1-5 RS-485 rate selection bits (see table below).
SW1-6 RS-485 rate selection bits (see table below).

SW1-5	**SW1-6**	**Baud Rate**
ON	ON	2400bps
ON	ON	4800bps
OFF	OFF	9600bps
OFF	OFF	19200bps

SW1



SW1-7 OPERATING MODE
When OFF, the output data remains scrambled and interleaved, allowing a direct connection to a MDT-3510 modulator for retransmission. This has significant benefits over simple IF to IF connection, since the output data has had the Viterbi FEC and Reed Solomon Correction applied. Hence the retransmitted signal will be far less likely to contain errors than a simple IF to IF connection.
When ON, the output data is deinterleaved and descrambled. It can be connected directly to an MPEG decoder. This is the normal operating position.

SW1-8 INCLUDE FLAGGED ERRORED PACKETS IN BER COUNT
When ON, flagged uncorrected packets are not included as an error in BER count. When OFF, flagged uncorrectable packets are added to any detected uncorrected packets to make the BER count. This switch has no impact on the received data output, only on the BER measurement data. It allows the user to ignore errors that were detected and marked as such by a receiver earlier in the transmission chain.

Jumper LK1

When shorted this link will hold the microcontroller IC23 in reset. This is useful while configuring switches SW1-SW5, since the positions of these switches are read by the micro only at power-on. Shorting LK1 briefly will emulate this condition without removing the power supply.

Note: This link should be left open circuit during normal operation.

Jumper LK2

When shorted this link will connect a terminating resistance of 220ohms across the RS-485 interface. This link should be installed when the module is the last in a series of daisy-chained modules, or if a long cable connection is used.

Installation

Pre-installation:

Handling:

This equipment may contain or be connected to static sensitive devices and proper static free handling precautions should be observed.

Where individual circuit cards are stored, they should be placed in antistatic bags. Proper antistatic procedures should be followed when inserting or removing cards from these bags.

Power:

AC mains supply: Ensure that operating voltage of unit and local supply voltage match and that correct rating fuse is installed for local supply.

DC supply: Ensure that the correct polarity is observed and that DC supply voltage is maintained within the operating range specified.

Earthing:

The earth path is dependent on the type of frame selected. In every case particular care should be taken to ensure that the frame is connected to earth for safety reasons. See frame manual for details.

Signal earth: For safety reasons a connection is made between signal earth and chassis earth. No attempt should be made to break this connection.

Installation in frame or chassis:

See details in separate manual for selected frame type.

RF Output and Intput:

RF Output and Input to each of the MDT-3510 and MDR-3510 respectively are via 75 Ω BNC connectors.

SPI Output and Input:

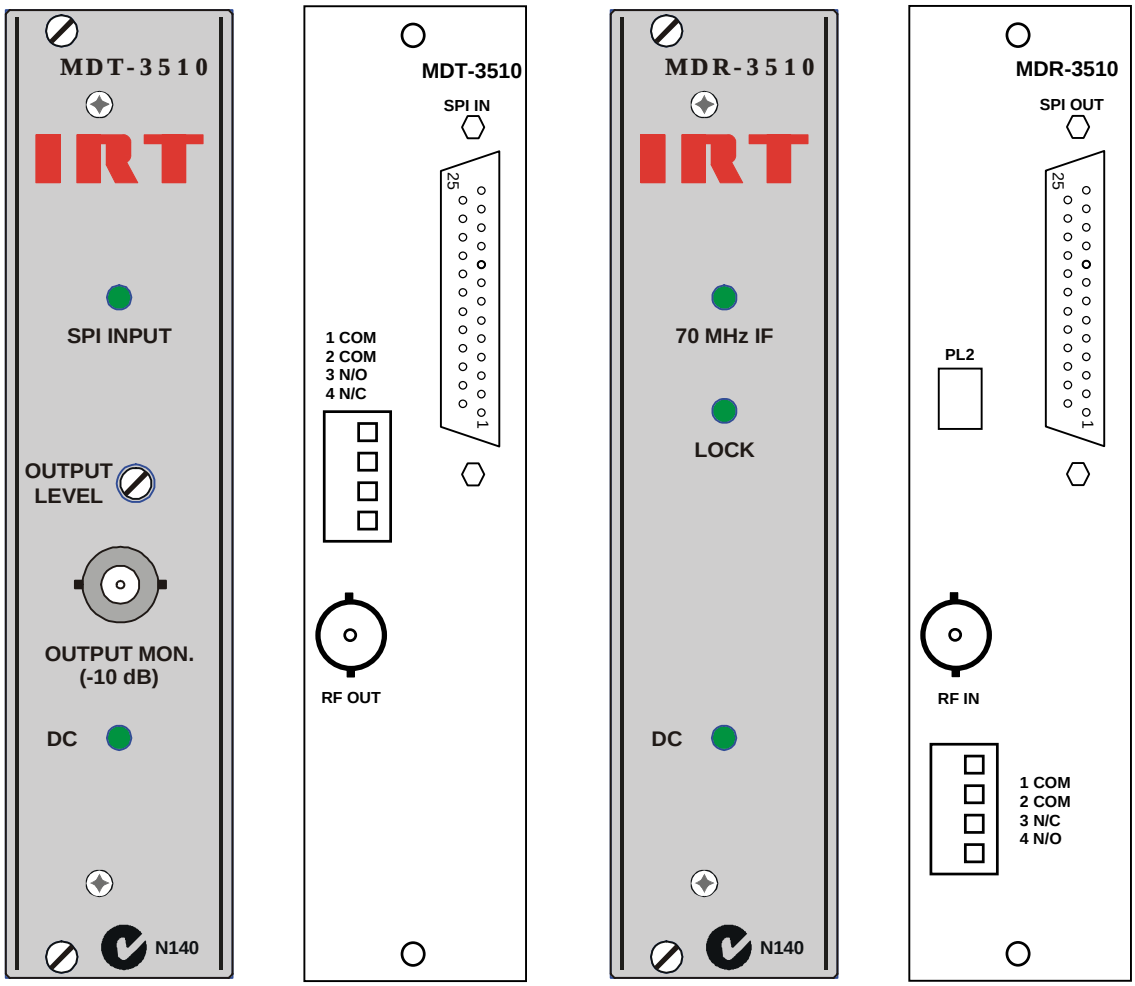
SPI Input and Output to each of the MDT-3510 and MDR-3510 respectively are via D25M connectors wired to the DVB SPI standard. The rear connector units of both the MDT-3510 and MDR-3510 both have D25F connectors for the SPI ports.

Alarm Output:

Both the MDT-3510 and the MDR-3510 have a 4 pin phoenix screw style connector for alarm outputs. See relevant pin details in Transmitter Interface and Receiver Interface sections.

Front & rear panel connector diagrams

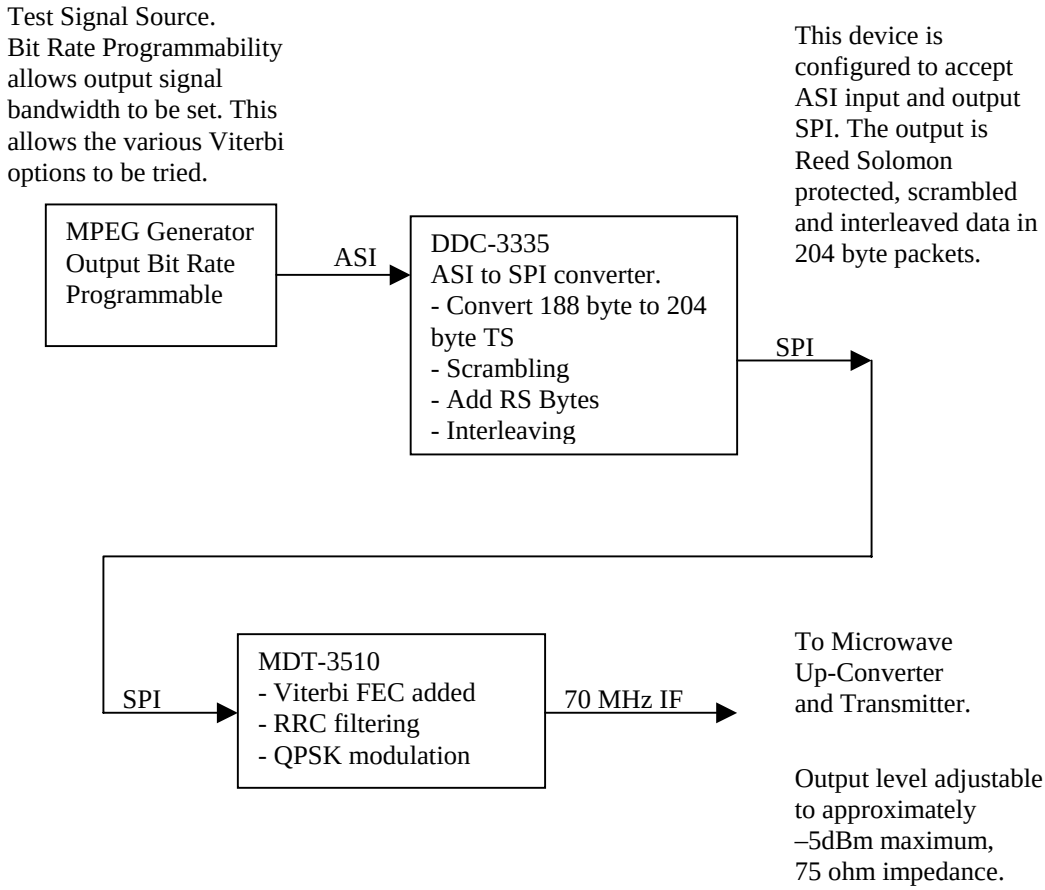
The following front panel and rear assembly drawings are not to scale and are intended to show connection order and approximate layout only.



Operation

Suggested System Configuration:

The Transmitter Interface:



RF Output Level Adjust:

The Potentiometer RV1 allows the user to adjust the RF output level by more than 30dB, to a maximum level of -5dBm. The Output Level Monitor 75ohm BNC on the front panel allows a spectrum analyzer or RF Power meter to be connected, allowing the level to be adjusted with the module installed in situ. Note that the Output Level Monitor connector is nominally -10dB with respect to the rear ancillary output level.

SPI Input LED:

This LED will be lit when the input SPI signal and Viterbi FEC selection result in a QPSK signal with symbol rate between 12 Msymbols/s to 28 Msymbols/s.

Symbol Rate = 1/2 x (Input 204 byte Packet Data Rate) x (1/Viterbi)

Hence for an input SPI rate of 34.368Mbps and a Viterbi FEC of 3/4

Symbol Rate = 1/2 x 34368000 x 4/3
= 22.912 MSymbols/s

Note that a 188 byte packet ASI signal at 31.672Mbps will result in a 204byte SPI signal at 34.368Mbps because of the extra 16 Reed Solomon bytes added to every packet.

(Input 204 byte Packet Data Rate) = (204/188) x (Input 188 byte Packet Data Rate)

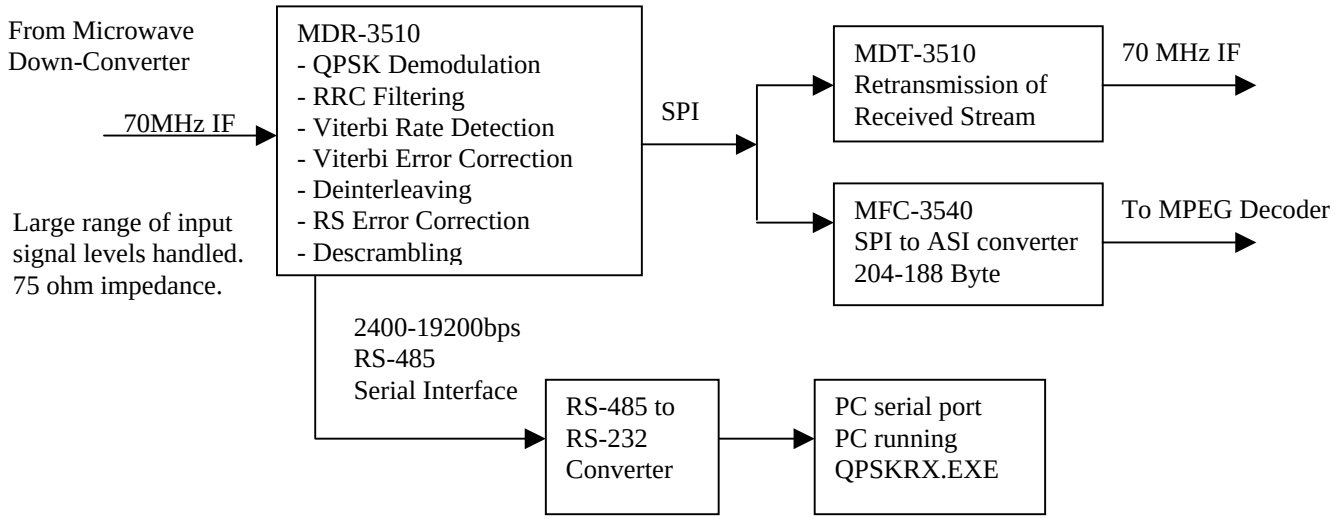
For a more detailed information, see the “Relation of Data Rate to Channel Bandwidth” section.

Relay Output J1 on Rear Assembly

This provides the user with 4 pins.

Pin 3 N/O - This pin is connected to COM when the SPI INPUT led is lit
Pin 4 N/C - This pin is connected to COM when power is off or the SPI INPUT led is not lit.
Pins 1 & 2 COM (2 pins) – Common pin that connects directly to N/O and N/C under the above conditions.

The Receiver Interface:



Note:

When a multiple hop microwave system is used, a retransmission link can be configured using just an MDR-3510 and MDT-3510 in a single rack unit. This allows correction and removal of errors on each individual link. A simple IF to IF link will allow potential errors to accumulate meaning more packets will be lost. When used in this configuration, set SW1-7 to OFF.

The Reed Solomon correction algorithm will correct up to 8 bytes in error every 204 byte packet. If there are more than 8 bytes in error the packet is marked as “uncorrectable” and is effectively lost by the system (a decoder will ignore this packet and rely on error concealment software to hide it from the end-viewer).

70MHz IF LED

This LED will be on when a carrier is detected at 70MHz, after AGC. The receiver has around 40dB of gain control and so will tolerate a large range of input RF levels.

LOCK LED

This LED will be on when a carrier is detected and the receiver has locked to the QPSK signal. This requires the Carrier Tracking Loop, and the Viterbi decoder, and the Reed Solomon decoder to be locked.

Relay Output PL4 on Rear Assembly

This provides the user with 4 pins.

Pin 4 N/O – This pin is connected to COM when the LOCK led is lit
Pin 3 N/C – This pin is connected to COM when power is off or the LOCK led is not lit.
Pins 1 & 2 COM (2 pins) – Common pin that connects directly to N/O and N/C under the above conditions.

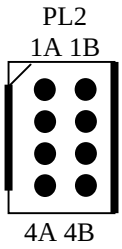
Computer Monitoring via RS-485 Interface

The "QPSKRX.EXE" program allows the user to record link errors, number of packets received, loss of synchronism and test duration. Start time is also recorded, so the exact time errors occurred can be determined. The errors are cumulative, and logged to the file "results.txt" so that it can be left running unattended for long periods of time.

The program counts uncorrectable errored packets. These are 204 byte packets in which more than 8 bytes are in error (after Viterbi), and hence the Reed Solomon algorithm cannot correct all the errors. These packets are therefore ignored by any MPEG decoder, and hence effectively lost.

The number of packets received allows an effective BER to be determined.

The Loss of Synchronism is incremented whenever a certain period without packets being received occurs. This effectively indicates that any data being transmitted at the moment has been lost, indicating serious path problems. It also prevents good BER measurements being obtained when serious errors cause system synchronism to be lost.



For connections to the RS-485 line, wire pins from PL2 to a DB9 Female connector as follows:

PL2	**DB9F**
3A	8 TXB
3B	3 TXA
4A	4 Ground

The serial data is transmitted as 8 bit data bytes with 1 start bit, 1 stop bit and no parity. The MSB is sent first. Each transmission comprises a packet of 7 bytes, and is initiated automatically when either the packet counter or sync loss counters hit their threshold values.

Threshold Value for packet number counter = 65536
Threshold Value for sync loss counter = 4095

The serial data packet transmitted via the RS-485 interface is comprised of the following:

Byte 1 – Address Byte

B7	B6	B5	B4	B3	B2	B1	B0
0	1	0	0	ADD3	ADD2	ADD1	ADD0

ADD3-ADD0 are set by SW1-1, SW1-2, SW1-3 and SW1-4 as defined above.

Byte 2 – Count Byte

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	0	1	1	0

Since a fixed length transmission, this byte is always the same, and corresponds to the number of bytes in the packet, not including the address byte.

Byte 3 – Error1 Byte

B7	B6	B5	B4	B3	B2	B1	B0
ERR15	ERR14	ERR13	ERR12	ERR11	ERR10	ERR9	ERR8

This byte consists of the 8 MSBs of the error count

Byte 4 – Error2 Byte

B7	B6	B5	B4	B3	B2	B1	B0
ERR7	ERR6	ERR5	ERR4	ERR3	ERR2	ERR1	ERR0

This byte consists of the 8 LSBs of the error count. The error count is incremented whenever a packet has more errors than can be handled by the Reed Solomon decoder (more than 8 bytes in error). This packet will be marked as uncorrectable, and any data it contains will be ignored by a decoder.

Byte 5 – Sync1 Byte

B7	B6	B5	B4	B3	B2	B1	B0
0	0	0	0	SL11	SL10	SL9	SL8

This byte consists of the 4 MSBs of the sync loss period count

Byte 5 – Error2 Byte

B7	B6	B5	B4	B3	B2	B1	B0
SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0

This byte consists of the 7 LSBs of the sync loss period count.

Note that a sync loss period is defined as a 416 micro second interval during which the system receiver cannot lock to the input QPSK signal. The output will be invalid during this period.

Byte 6 – Checksum Byte

B7	B6	B5	B4	B3	B2	B1	B0
CHK7	CHK6	CHK5	CHK4	CHK3	CHK2	CHK1	CHK0

The checksum byte is used to determine the validity of the packet. If Bytes 1-5 are added to the Checksum byte the result should be 0 modulo 256. Any other result indicates a serial data transmission error has occurred.

Basic Troubleshooting

1. DC LED not lit

- Power supply not on or faulty
- LED not functional.

2. 70MHz IF LED not lit

- No RF input signal present
- RF input level too low
- IF frequency not 70MHz
- LK1 is installed. This will hold the board in Reset and should be removed.

3. LOCK LED not lit but 70MHZ IF LED is

- Incorrect Symbol Rate selected on Switches SW2-SW5. Remember
- Symbol Rate = 1/2 x (204 byte Bit Rate) x (1/Viterbi Rate)

  Also remember that the Bit Rate corresponds to the serial data rate of the 204 byte packet stream.
- Data stream has not undergone energy dispersal (scrambling) prior to modulation at the transmitter end.
- Data stream has not undergone interleaving prior to modulation at the transmitter end.
- Data stream has not had Reed Solomon checksum bytes added prior to modulation at the transmitter end.
- Data stream input to modulator at transmitter end is 188 byte packet length not 204 byte (hence no Reed Solomon checksum bytes).
- Data stream and Viterbi selection may generate an IF signal that is too wide for the microwave link IF filters. Reduce Viterbi Rate or Data rate at transmit end and change symbol rate switches accordingly on receiver board.
- LK1 is installed. This will hold the board in Reset and should be removed.

4. All front panel LEDs are on but equipment connected to SPI output not working.

- SW1-7 is OFF. This switch configures the board into a retransmission or link mode. In this situation, the SPI output is still scrambled and interleaved with Reed Solomon bytes (suitable for direct connection to another modulator MDT-3510). It is still a valid transport stream, but most MPEG decoders will not like this signal. Turn SW1-7 ON.
- High error rate. Check the RS-485 interface BER results. Change Viterbi rate at transmit end or reduce data rate. Verify link integrity.

5. All front panel LEDs on but RS-485 interface not working

- Check selected baud rate (SW1-5 and SW1-6) is correct.
- Install LK2 if receiver is at the end of long RS-485 cable.
- Verify that RS-485 signal is present and not badly attenuated. Remove LK2 if this is the case.

Maintenance & storage

Maintenance:

No regular maintenance is required.

Care however should be taken to ensure that all connectors are kept clean and free from contamination of any kind. This is especially important in fibre optic equipment where cleanliness of optical connections is critical to performance.

Storage:

If the equipment is not to be used for an extended period, it is recommended the whole unit be placed in a sealed plastic bag to prevent dust contamination. In areas of high humidity a suitably sized bag of silica gel should be included to deter corrosion.

Where individual circuit cards are stored, they should be placed in antistatic bags. Proper antistatic procedures should be followed when inserting or removing cards from these bags.

Warranty & Service

Equipment is covered by a limited warranty period of three years from date of first delivery unless contrary conditions apply under a particular contract of supply. For situations when "**No Fault Found**" for repairs, a minimum charge of 1 hour's labour, at IRT's current labour charge rate, will apply, whether the equipment is within the warranty period or not.

Equipment warranty is limited to faults attributable to defects in original design or manufacture. Warranty on components shall be extended by IRT only to the extent obtainable from the component supplier.

Equipment return:

Before arranging service, ensure that the fault is in the unit to be serviced and not in associated equipment. If possible, confirm this by substitution.

Before returning equipment contact should be made with IRT or your local agent to determine whether the equipment can be serviced in the field or should be returned for repair.

The equipment should be properly packed for return observing antistatic procedures.

The following information should accompany the unit to be returned:

1. A fault report should be included indicating the nature of the fault
2. The operating conditions under which the fault initially occurred.
3. Any additional information, which may be of assistance in fault location and remedy.
4. A contact name and telephone and fax numbers.
5. Details of payment method for items not covered by warranty.
6. Full return address.
7. For situations when "**No Fault Found**" for repairs, a minimum charge of 1 hour's labour will apply, whether the equipment is within the warranty period or not. Contact IRT for current hourly rate.

Please note that all freight charges are the responsibility of the customer.

The equipment should be returned **to the agent who originally supplied the equipment** or, where this is not possible, to IRT direct as follows.

Equipment Service
IRT Electronics Pty Ltd
26 Hotham Parade
ARTARMON
N.S.W. 2064
AUSTRALIA

Phone: 61 2 9439 3744 Fax: 61 2 9439 7439
Email: service@irtelectronics.com

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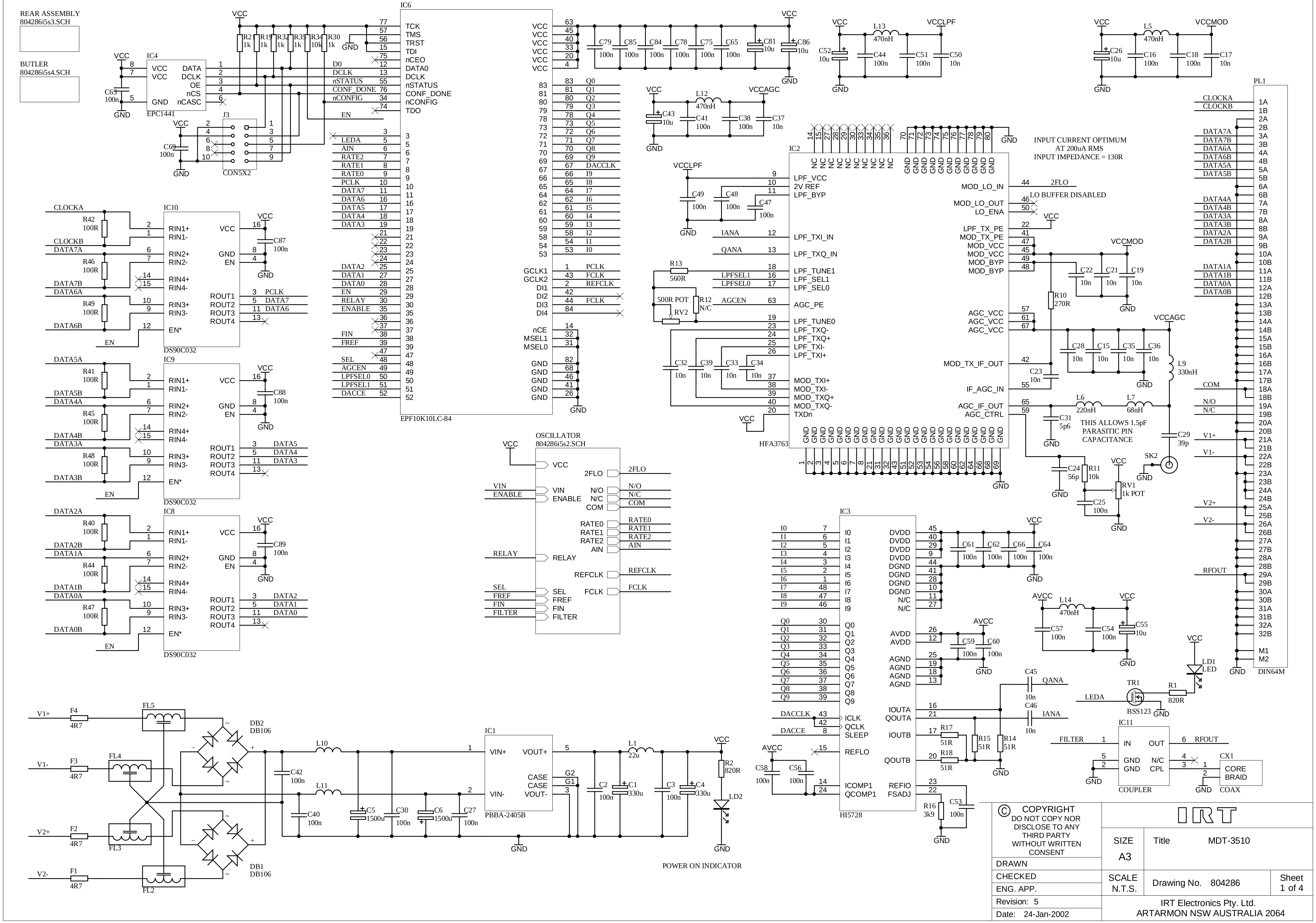
804286	4	MDT-3510 QPSK Modulator 70 MHz IF circuit
804288	1	MDR-3510 QPSK Demodulator 70 MHz IF circuit
804288	2	MDR-3510 QPSK Demodulator 70 MHz IF circuit
804288	3	MDR-3510 QPSK Demodulator 70 MHz IF circuit
804288	4	MDR-3510 QPSK Demodulator 70 MHz IF circuit
804288	5	MDR-3510 QPSK Demodulator 70 MHz IF circuit



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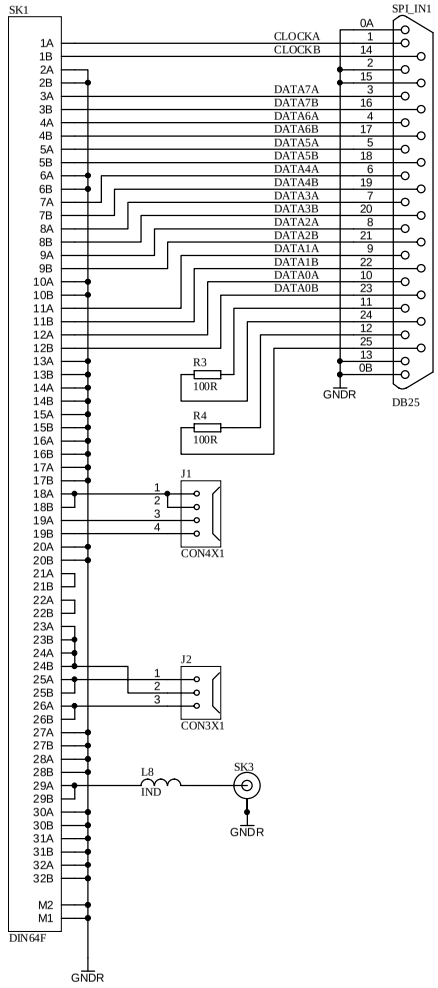

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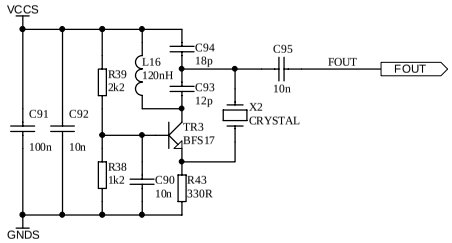

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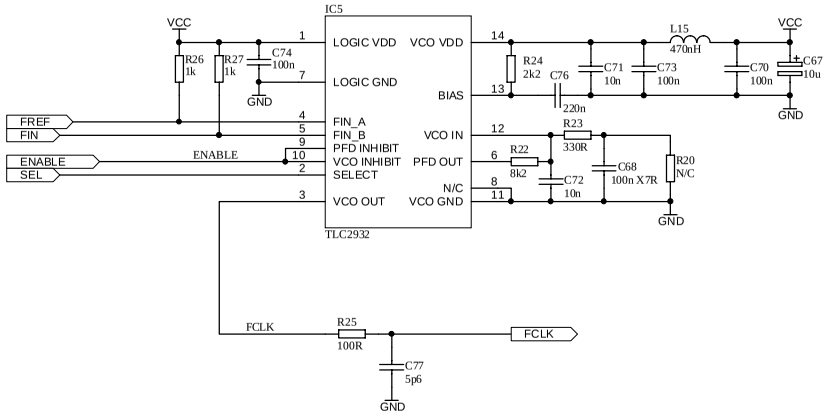
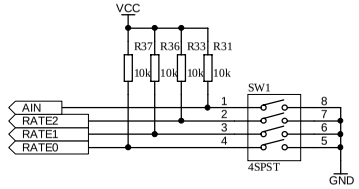
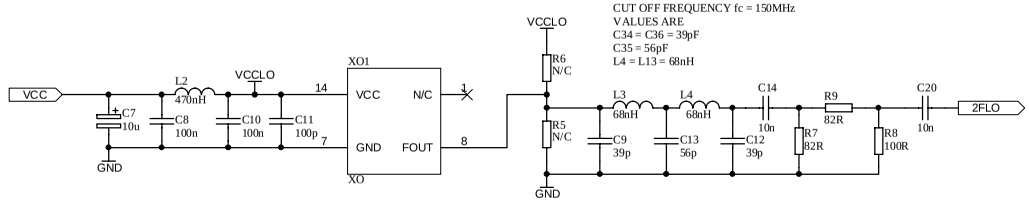
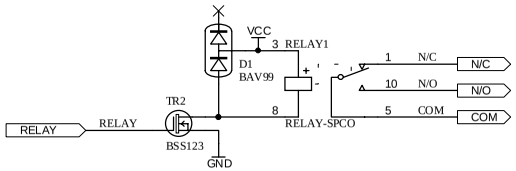
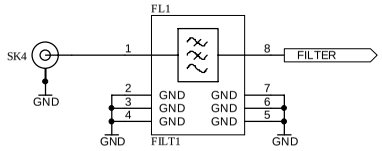


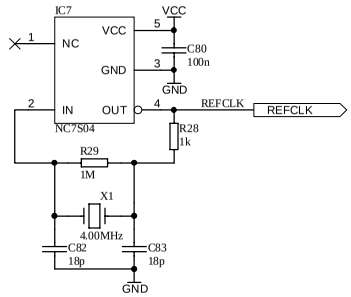




THIS RESISTOR PAD ASSUMES
BUTLER CRYSTAL OSCILLATOR
CIRCUIT IS USED.
FOR HIGHER OUTPUT POWER
CRYSTAL OSCILLATOR MODULES,
THESE RESISTOR
VALUES MAY NEED TO BE CHANGED
TO REDUCE LEVEL INPUT TO THE
HFA3763







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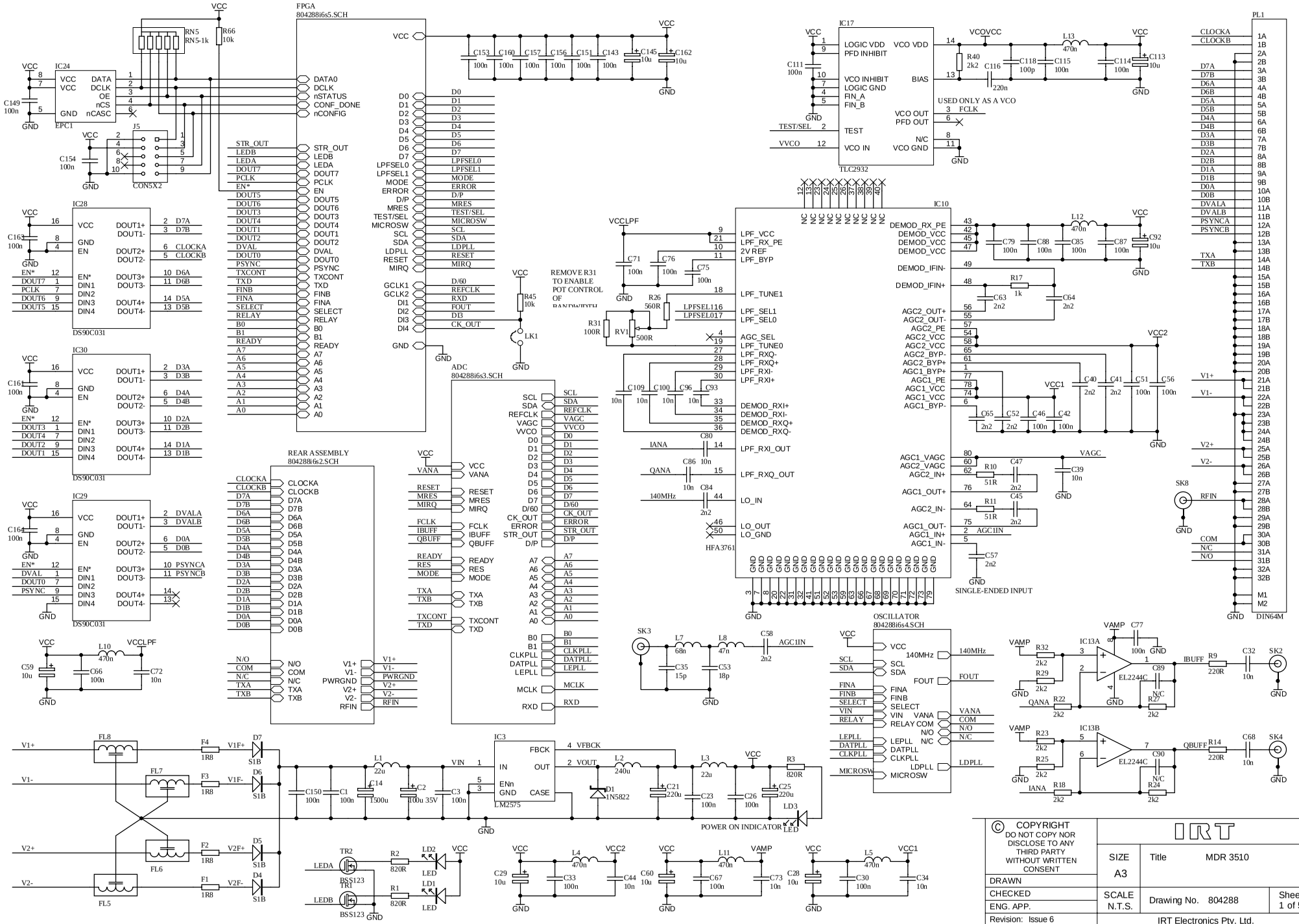
FPGA
804288i6s5.SCH
IC17
TLC2932
PL1
IC10
HFA3761
IC28
IC30
IC29
DS90C031
EPC1
IC24
J5
CON5X2
REAR ASSEMBLY
804288i6s2.SCH
ADC
804288i6s3.SCH
OSCILLATOR
804288i6s4.SCH
IC3
LM2575
REMOVE R31
TO ENABLE
POT CONTROL
OF
SINGLE-ENDED INPUT
POWER ON INDICATOR
USED ONLY AS A VCO
IRT
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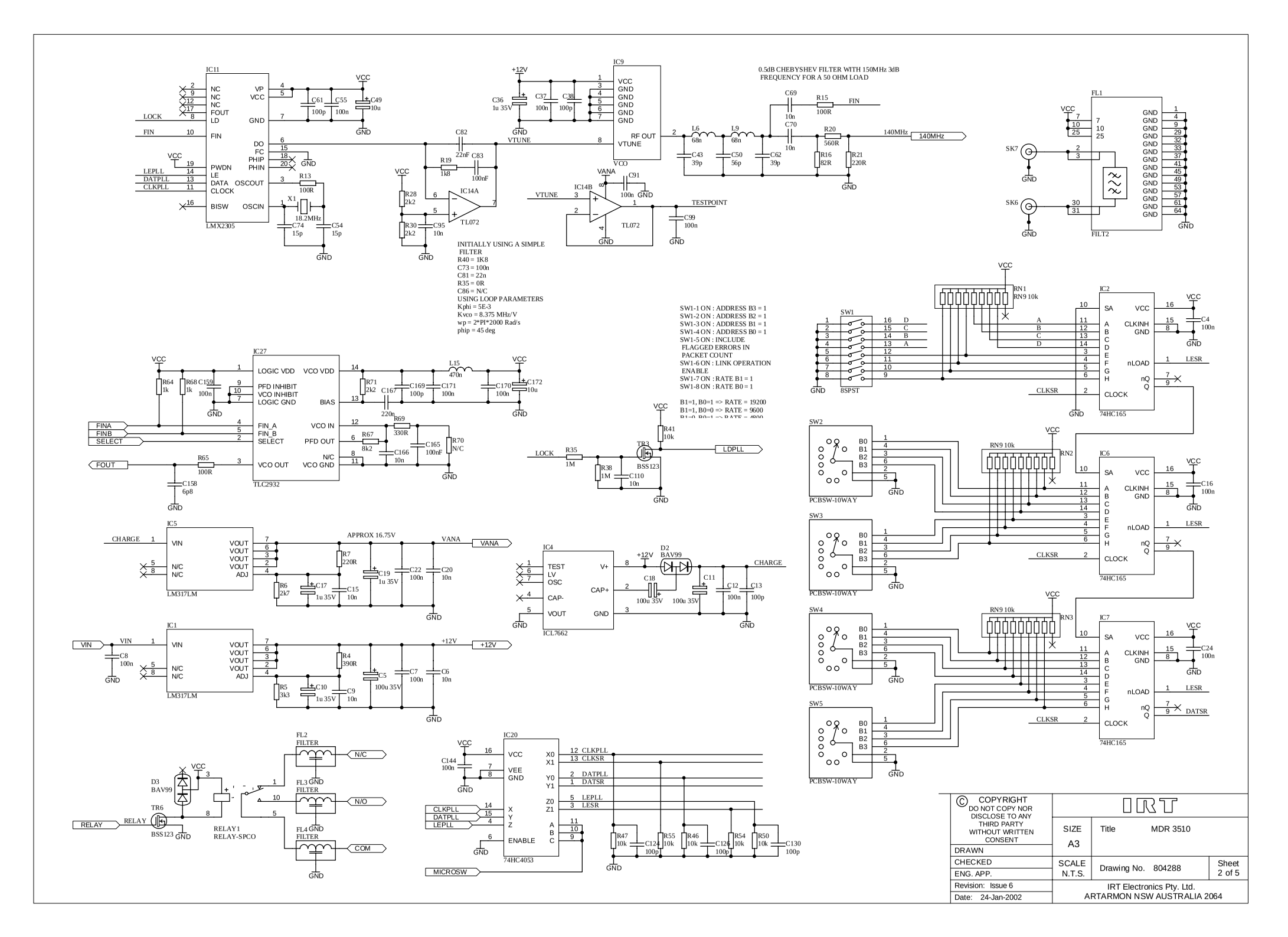

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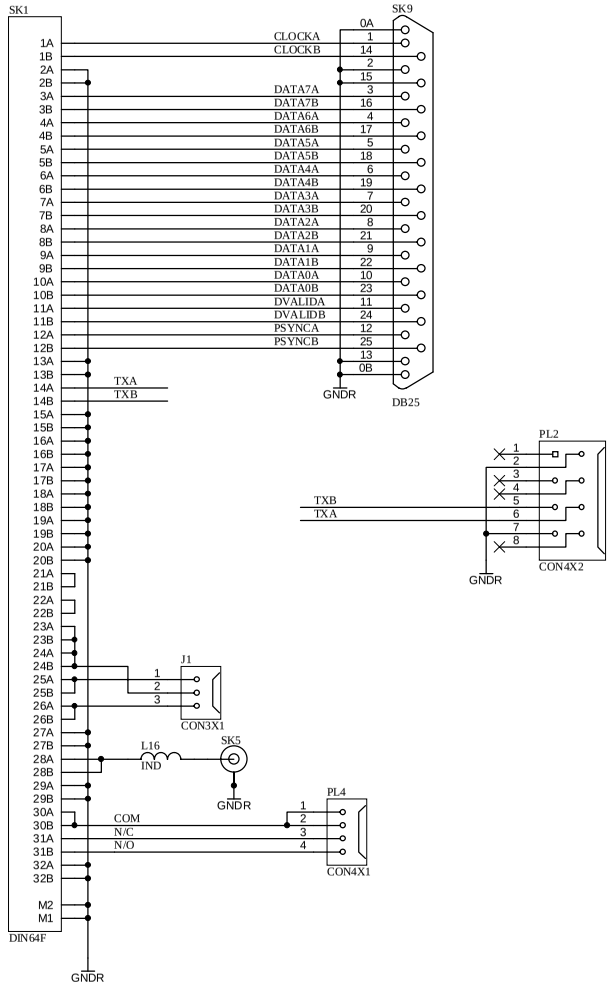

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	SIZE A3	Title MDR 3510	
DRAWN			
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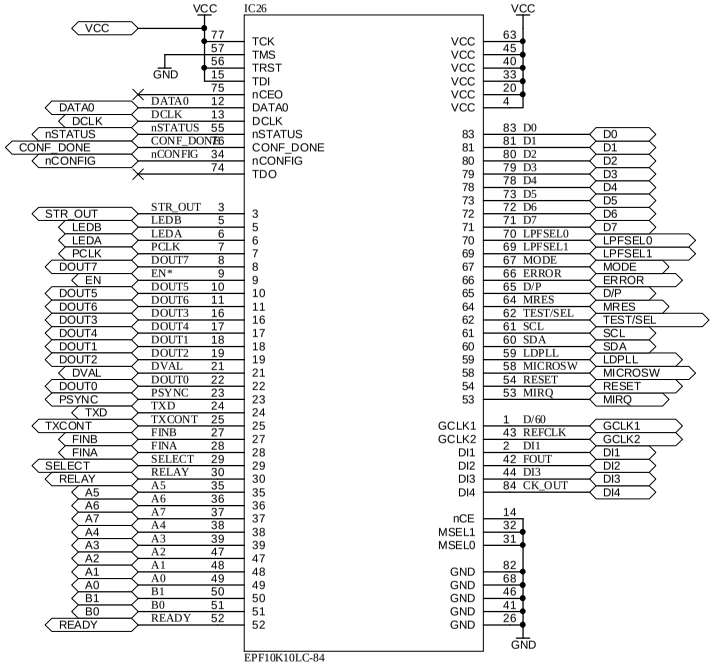

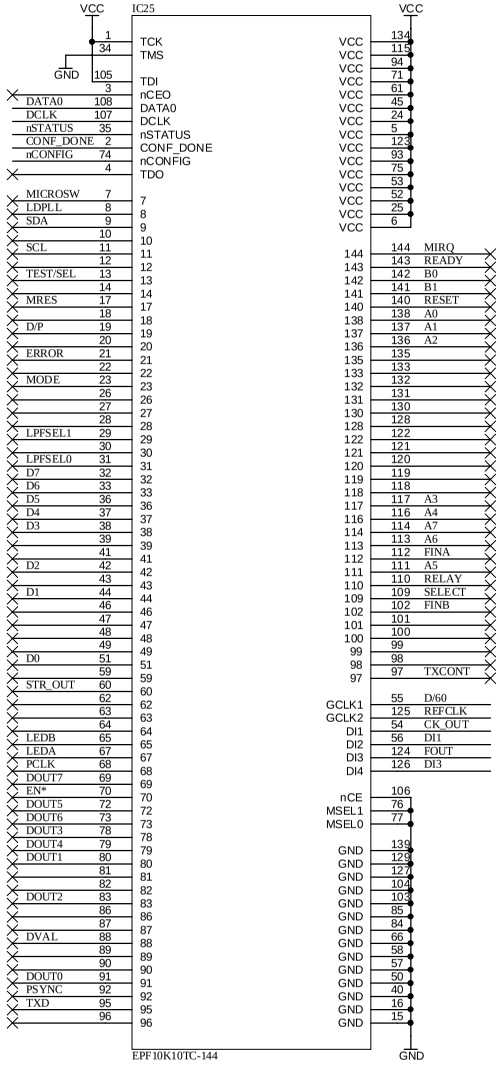

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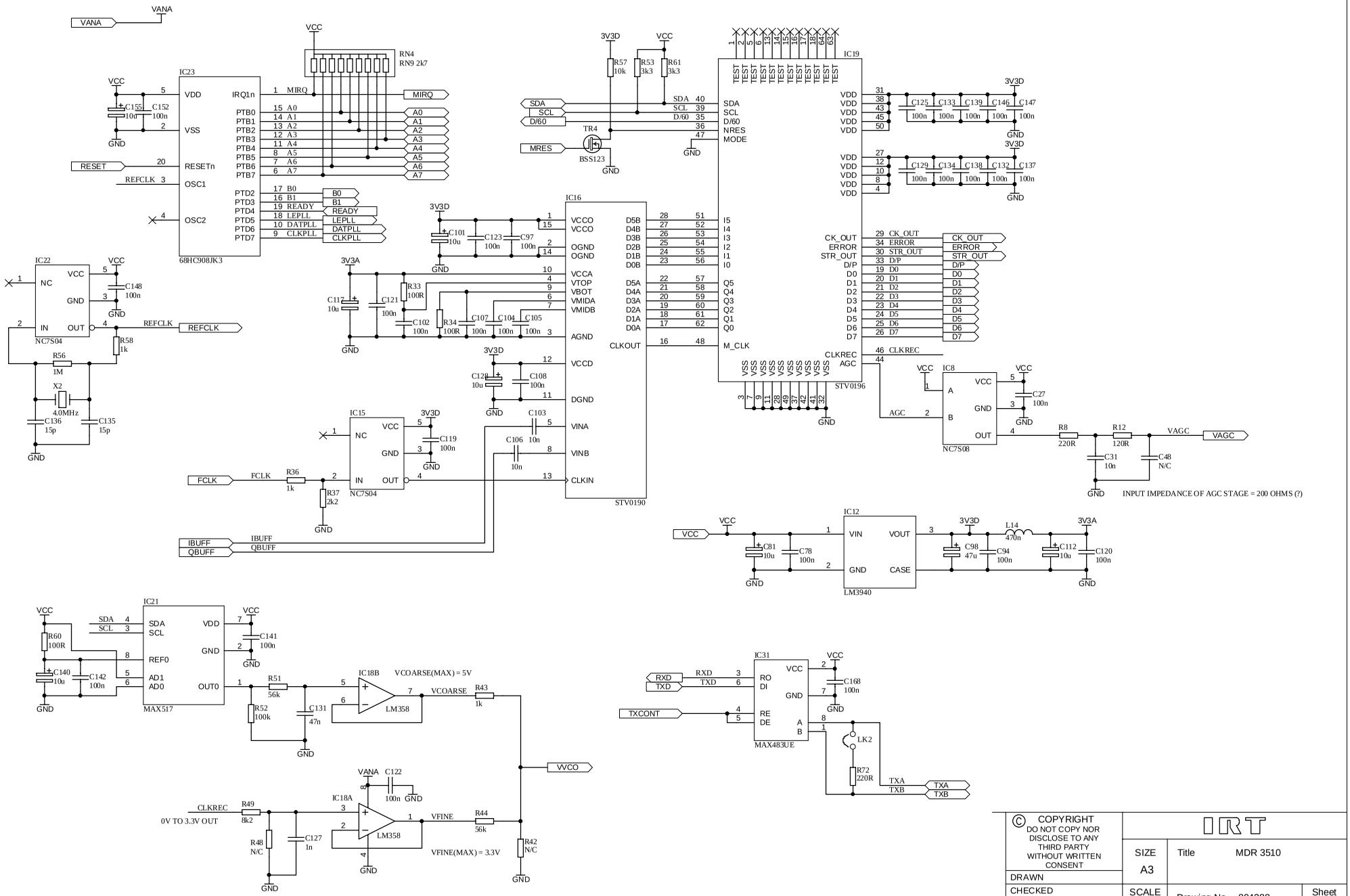

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