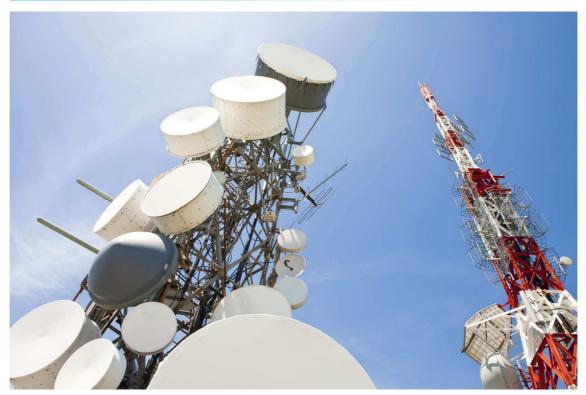


G.703 to ASI Network Interface Adapter





User Manual

Revision History:

Revision	Date	Ву	Change Description	Applicable to:
00	19/11/2004	AL	Original Issue.	Firmware version ≥ MDR3670i1B (22/11/2004)
01	05/11/2009	AL	"Special" Rate dropped, now compatible with older MFC-3485	Firmware version ≥ MDR3670i1C (11/12/2009)
02	14/07/2010	AL	Rev. 0 and Rev. 1 handbooks combined to reflect differences in firmware versions. ASI output mode, burst or continuous, added.	Firmware versions MDR3670i1B (22/11/2004) or MDR3670i1C (11/12/2009)
03	11/10/2010	AL	Firmware version MDR3670i1D DIP switch settings (SW4-3 and SW4-7) added.	Firmware versions MDR3670i1B (22/11/2004), MDR3670i1C (11/12/2009) or MDR3670i1D (15/09/2010)
04	24/01/2012	AL	SW4-3 DIP switch setting corrected for firmware i1D version.	Firmware versions MDR3670i1B (22/11/2004), MDR3670i1C (11/12/2009) or MDR3670i1D (15/09/2010)
05	24/05/2012	AL	Reformatted layout.	Firmware versions MDR3670i1B (22/11/2004), MDR3670i1C (11/12/2009) or MDR3670i1D (15/09/2010)

Table of Contents:

Section	Page
Revision History	2
Operational Safety	3
General Description	4
Technical Specifications	5
Technical Description	6
Configuration	7
Installation	8
Front and rear layouts	9
Operation	10
Front panel indicators	10
Processing controls	11
Maintenance & Storage	12
Warranty & Service	12
Equipment return	12
Characteristics of Signal Types	13
Coding characteristics	13
G.703	13

This instruction book applies to units programmed with firmware version MDR3670i1B, MDR3670i1C or MDR3670i1D.

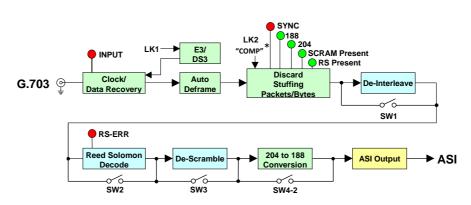
OPERATIONAL SAFETY

WARNING

Operation of electronic equipment involves the use of voltages and currents that may be dangerous to human life. Note that under certain conditions dangerous potentials may exist in some circuits when power controls are in the **OFF** position. Maintenance personnel should observe all safety regulations.

Do not make any adjustments inside equipment with power **ON** unless proper precautions are observed. All internal adjustments should only be made by suitably qualified personnel. All operational adjustments are available externally without the need for removing covers or use of extender cards.

BLOCK DIAGRAM MDR-3670 SIGNAL PATH



* Compatible Mode

The MDR-3670 is part of a family of data transcoders for converting between the commonly used MPEG2 Transport Stream formats in the broadcast industry for video distribution.

The MDR-3670 operates with either an E3 (34.368 Mb/s) or DS3 (44.736 Mb/s) G.703 rates.

There are several industry modes of encoding that can be decoded by the MDR-3670. They are loosely classified as follows:

Standard: IRT MDT-3570, DDC-3480.

Upstream: Similar to above. Downstream: Packet stuffed.

Compatible: Legacy Framing (firmware version MDR3670i1B).

9 bit decoding, IRT MFC-3485 (firmware versions MDR3670i1C & MDR3670i1D).

This range covers most other manufacturer's equipment.

Front panel switches allow Reed Solomon correction and/or the removal of interleaving and scrambling (energy dispersal). On board switches allow 204 to 188 conversion, after decoding.

The MDR-3670 is fabricated in IRT's standard Eurocard format and may be housed in a variety of IRT's frames.

Standard features:

- Wide Range of G.703 to ASI conversions
- E3 or DS3 operation with automatic DS3 De-framing
- Reed Solomon correction
- De-interleaving
- De-scrambling
- Packet length indication

TECHNICAL SPECIFICATIONS

Inputs:

Type $1 \times G.703$, 75Ω BNC connector.

G.703 Rate E3 (34.368 Mb/s) or DS3 (44.736 Mb/s), link selectable.

Outputs:

Type 1 x ASI-C 75Ω , 800 mVp-p, BNC connector.

Mode Continuous or Burst, DIP switch settable (firmware versions MDR3670i1B &

MDR3670i1D).

Burst (firmware version MDR3670i1C).

Alarms:

Major Relay NO/NC link selectable,

(Relay energised when Input Sync is obtained).

Minor Relay NO/NC link selectable,

(Relay energised when there are no Reed Solomon Errors).

Power Requirements:

Voltage 28 Vac CT (14-0-14) or \pm 16 Vdc.

Power consumption < 5.5 VA.

Other:

Temperature range 0 - 50° C ambient.

Mechanical Suitable for mounting in IRT 19" rack chassis with input, output and power connections

on the rear panel.

Finish: Front panel Grey background, black lettering & red IRT logo.

Rear assembly Detachable silk-screened PCB with direct mount connectors to Eurocard and

external signals.

Dimensions 6 HP x 3 U x 220 mm IRT Eurocard

Supplied accessories Rear connector assembly including matching connector for alarm output.

Revision 05

The MDR-3670 converts an appropriate G.703 input to an ASI-C signal.

This module is capable of performing de-scrambling, RS decoding and de-interleaving. Certain combinations of functions are inhibited (e.g. de-interleaving of a 188 byte transport stream).

The processing functions are selected using three switches (de-scrambling, RS decoding and de-interleaving) on the front panel. Each switch has two positions (up or down).

A switch set to the UP position enables the decoding section.

A switch set to the DOWN position bypasses the decoding section.

ASI Output

ASI operates at 270 Mb/s and uses 8B/10B coding with K28.5 stuffing bytes. The ASI cable output uses a 75 Ohm BNC connector. An ASI optical link can be used to transport the ASI-C signal via fibre optic cable. See IRT Fibre link brochures or manuals for further information.

Alarm relays

Major Alarm ("Loss of Sync") and Minor Alarm ("RS Errors") relay contacts are available on PL4 of the rear assembly. N/O or N/C contacts to ground are selected by link settings LK5 and LK6.

LED indicators

LED indicators 188 TS Byte length, 204 TS Byte length, RS error, Scram present, RS present are blanked during Input loss or sync loss.

Link settings:

Warning:

Links may be changed without disconnecting power. However, when any link is changed, normal decoding of the MPEG TS will be disturbed. The time taken before normal decoding resumes is dependent on the decoder in use and may be up to five seconds.

LK1 - IN: selects E3 operation (34.368 Mb/s).
OUT: selects DS3 operation (44.736 Mb/s).

LK2 - IN: selects "compatible" mode of operation for compatibility with some other manufacturer's older style of encoding (firmware version MDR3670i1B).

OUT: selects standard mode of operation (firmware version MDR3670i1B).

LK2 - IN: selects 9-bit "compatible" mode of operation for compatibility with IRT's MFC-3485 (firmware versions MDR3670i1C & MDR3670i1D).

OUT: selects standard mode of operation (firmware versions MDR3670i1C & MDR3670i1D).

LK3 - not used LK4 - not installed

LK5 - with link in position A then Major Alarm relay output is configured to be "normally closed",

with link in position B then Major Alarm relay output is configured to be "normally open".

LK6 - with link in position A then Minor Alarm relay output is configured to be "normally closed", with link in position B then Minor Alarm relay output is configured to be "normally open".

LK7 - not installed

Note: "normally open" indicates with the relay energised, the output looks like an open circuit to ground.

With no power to the board, or with relay non-energized, the relay output is short circuit to ground.

Major Alarm - relay energised when Input Sync obtained.

Minor Alarm - relay energised when there are no RS errors.

Switch settings:

SW4-1 - not used.

SW4-2 ON - 204 to 188 byte conversion enabled SW4-2 OFF - 204 to 188 byte conversion disabled

SW4-3 ON - Payload data¹ is evenly distributed (continuous) in ASI output (f/w version MDR3670i1B).
SW4-3 OFF - Payload data¹ in each packet is contiguous (burst) in ASI output (f/w version MDR3670i1B).

SW4-3 - not used (firmware version MDR3670i1C).

SW4-3 ON - Payload data¹ is evenly distributed (continuous) in ASI output (f/w version MDR3670i1D).
 SW4-3 OFF - Payload data¹ in each packet is contiguous (burst) in ASI output (f/w version MDR3670i1D).
 SW4-4 ON - TEI² bit (Transport Error Indicator) set in outgoing stream if an uncorrectible error is detected.

SW4-4 OFF - TEI² bit (Transport Error Indicator) in outgoing stream is unchanged.

SW4-5 ON - R-S led shows both correctible and uncorrectible errors

SW4-5 OFF - R-S led shows uncorrectible errors only.

SW4-6 - not used

SW4-7 - not used (firmware versions MDR3670i1B & MDR3670i1C).

SW4-7 ON - ASI output continues for several hundredths of a ms after loss of G.703 input³ (firmware version MDR3670i1D).

SW4-7 OFF - Normal ASI output behaviour on loss of G.703 input (firmware version MDR3670i1D).

SW4-8 ON - Receiver equaliser (G.703) disabled SW4-8 OFF - Receiver equaliser (G.703) enabled

NOTE: 1 ASI output payload data is only contiguous (burst) with firmware version MDR3670i1C.

2 TEI – b7 of byte after sync byte.

3 This ensures that a downstream DDA-3310 will see a loss of ASI and switch even for rates down to 1.2Mb/s (firmware version MDR3670i1D).

Pre-installation:

Handling:

This equipment may contain or be connected to static sensitive devices and proper static free handling precautions should be observed.

Where individual circuit cards are stored, they should be placed in antistatic bags. Proper antistatic procedures should be followed when inserting or removing cards from these bags.

Power:

AC mains supply: Ensure that operating voltage of unit and local supply voltage match and that correct rating

fuse is installed for local supply.

DC supply: Ensure that the correct polarity is observed and that DC supply voltage is maintained within

the operating range specified.

Earthing:

The earth path is dependent on the type of frame selected. In every case particular care should be taken to ensure that the frame is connected to earth for safety reasons. See frame manual for details.

Signal earth: For safety reasons a connection is made between signal earth and chassis earth. No attempt should be made to break this connection.

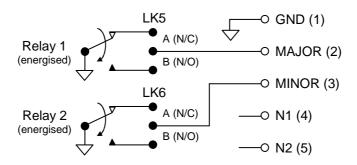
Installation in frame or chassis:

See details in separate manual for selected frame type.

Input/Output & alarm connections:

G.703 input and ASI output are by 75Ω BNC connectors on the rear assembly.

Alarm outputs are by a 5-pin Phoenix style screw connector on the rear assembly. Alarms are by relay contacts. Links LK5 and LK6 set the Major Alarm (Relay 1) and the Minor Alarm (Relay 2) to be N/O or N/C to ground.



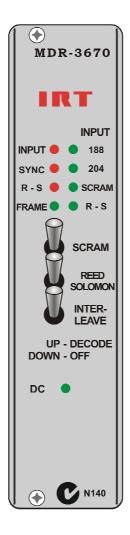
The Major Alarm condition is "Loss of Sync".

The Minor Alarm condition is "RS Errors".

N1 – not connected.

N2 – not connected.

Front & rear panel connector diagrams:





OPERATION

The MDR-3670 operates in a G.703 to ASI decode mode. The three front panel switches determine the decoding operations performed. Not all combinations of decoding are valid or optimal for use with MPEG2 transport streams. The user must be aware of the intended application and the Transport Stream format used.

Switches in the UP position apply decoding and switches in the DOWN position bypass decoding.

The application of certain processing functions is automatically blocked if the incoming stream is not in a suitable format, e.g. if the incoming Transport Stream contains 188 Byte packets then neither De-Interleaving nor Reed Solomon Decoding can be applied. The MDR-3670 provides a visual indication of the incoming Transport Stream format, e.g. Packet size 188/204, Scrambling or RS coding. These indicators help the user decide which processing functions are required.

TS Transmission Formats

The application of scrambling, interleaving and RS encoding is required prior to satellite or terrestrial modulators (e.g. QPSK modulation for satellite). Interleaving and RS coding are almost always used together. Interleaving reduces the impact of burst errors by redistributing the error burst over multiple packets. Since the RS decoder can only correct up to 8 bytes per packet, interleaving increases the likelihood of all the errors being corrected. If a packet has more than 8 error bytes, an RS decoder will be unable to correct that packet. Scrambling or energy dispersal on the other hand eliminates long strings of '1's or '0's, and hence helps maintain the DC balance of the transmitted signal.

Front Panel Indicators:

Input loss alarm:

This LED lights when G.703 loss of signal is detected.

Sync loss alarm:

This LED lights when a valid MPEG-2 TS is absent but G.703 signal is present.

SYNC 204 R-S SCRAM FRAME R-S

INPUT () 188

188 byte indicator:

This LED lights when a valid MPEG-2 TS with 188 byte packet length is decoded.

204 byte indicator:

This LED lights when a valid MPEG-2 TS with 204 byte packet length is decoded.

Scrambling presence indicator:

After decoding, this LED lights when a valid MPEG-2 TS stream containing a byte sequence that corresponds to scrambling. A scrambling byte sequence uses an inverted 47H sync byte (B8H) every eighth sync to signify the start of the scrambling sequence.

R-S (Reed Solomon) presence indicator (Green):

After decoding, this LED lights when Reed Solomon error correction bytes are present in place of the 16 dummy bytes of a 204 Byte MPEG-2 TS. The MDC-3470 considers any data content other than all 0's during the 16 dummy bytes to be RS correction bytes.

R-S (Reed Solomon) Error indicator (Red):

Depending on the position of switch SW4E, this LED lights for at least 300 ms when only un-correctable R-S packets are detected (SW4E-OFF), or either uncorrectable and correctable RS packets are detected (SW4E-ON). Uncorrectable errors correspond to packets with more than 8 bytes in error.

Frame indicator (Green):

This LED lights when the input G.703 signal is of a framed format (DS3 only).

Processing controls:

This module is capable of performing de-scrambling, RS decoding and de-interleaving.

In this context, the word scrambling refers to the process of randomisation for the purpose of energy dispersal of the signal. It does <u>not</u> refer to the encryption applied to Pay TV signals to control access to particular channels or programs.

The processing functions are selected using three switches (de-scrambling, RS decoding and de-interleaving) on the front panel. Each switch has two positions.

A switch set to the UP position applies processing to the decoding section, a switch set to the DOWN position does not perform that function.



UP - DECODE DOWN - OFF

NOTE: When being used in the 9-bit "compatible" mode with an MFC-3485 encoder, all front panel switches must be set to the OFF position (applicable to firmware versions MDR3670i1C & MDR3670i1D).

Maintenance:

No regular maintenance is required.

Care however should be taken to ensure that all connectors are kept clean and free from contamination of any kind. This is especially important in fibre optic equipment where cleanliness of optical connections is critical to performance.

Storage:

If the equipment is not to be used for an extended period, it is recommended the whole unit be placed in a sealed plastic bag to prevent dust contamination. In areas of high humidity a suitably sized bag of silica gel should be included to deter corrosion.

Where individual circuit cards are stored, they should be placed in antistatic bags. Proper antistatic procedures should be followed when inserting or removing cards from these bags.

WARRANTY & SERVICE

Equipment is covered by a limited warranty period of three years from date of first delivery unless contrary conditions apply under a particular contract of supply. For situations when "**No Fault Found**" for repairs, a minimum charge of 1 hour's labour, at IRT's current labour charge rate, will apply, whether the equipment is within the warranty period or not.

Equipment warranty is limited to faults attributable to defects in original design or manufacture. Warranty on components shall be extended by IRT only to the extent obtainable from the component supplier.

Equipment return:

Before arranging service, ensure that the fault is in the unit to be serviced and not in associated equipment. If possible, confirm this by substitution.

Before returning equipment contact should be made with IRT or your local agent to determine whether the equipment can be serviced in the field or should be returned for repair.

The equipment should be properly packed for return observing antistatic procedures.

The following information should accompany the unit to be returned:

- 1. A fault report should be included indicating the nature of the fault
- 2. The operating conditions under which the fault initially occurred.
- 3. Any additional information, which may be of assistance in fault location and remedy.
- 4. A contact name and telephone and fax numbers.
- 5. Details of payment method for items not covered by warranty.
- 6. Full return address.
- 7. For situations when "**No Fault Found**" for repairs, a minimum charge of 1 hour's labour will apply, whether the equipment is within the warranty period or not. Contact IRT for current hourly rate.

Please note that all freight charges are the responsibility of the customer.

The equipment should be returned to the agent who originally supplied the equipment or, where this is not possible, to IRT directly. Details of IRT's direct address can be found at IRT Electronics' website.

Web address: www.irtelectronics.com

Email: sales@irtelectronics.com

Coding characteristics

G.703:

The HDB3 (High Density Bi-polar of order 3) code as defined in G.703 for 34,368 kb/s is as follows:

Binary 1 bits are represented by alternate positive and negative pulses and binary 0 bits by spaces. Exceptions are made when strings of successive 0 bits occur in the binary signal.

Each block of 4 successive zeros is replaced by 000V or B00V where B is an inserted pulse of the correct polarity and V is an inserted pulse violating the polarity rule. The choice of 000V or B00V is made so that the number of B pulses between consecutive V pulses is odd so that successive V pulses are of alternate polarity and so no DC component is introduced.

The **B3ZS** (Bipolar with Three Zero Substitution) (also designated **HDB2** - High Density Bi-polar of order 2) code as defined in G.703 for 44,736 kb/s is as follows:

Binary 1 bits are represented by alternate positive and negative pulses and binary 0 bits by spaces. Exceptions are made when strings of successive 0 bits occur in the binary signal.

Each block of 3 successive zeros is replaced by 00V or B0V. The choice of 00V or B0V is made so that the number of B pulses between consecutive V pulses is odd, so that successive V pulses are of alternate polarity and so no DC component is introduced.